

# Final Program

April 20, 2016 Main Hall(7th Floor), Yokohama Joho Bunka Center  
(Yokohama Media & Communications Center)

**13:30-15:00**    **Special Invited Lecture 1**  
*Chair: Tohru Ishihara (Kyoto Univ.)*

13:30-15:00    **Inter/Intra-Chip Optical Networks**  
*Jiang Xu (Hong Kong Univ. of Science and Technology, China)*

**Abstract:** The performance and energy efficiency of a computing system is determined not only by its processors, memories, storage, and peripherals but also how efficiently they communicate with each other. As new applications continuously require more communication bandwidth, metallic interconnects gradually become the bottlenecks of computing systems due to their high power consumption, limited bandwidth, and signal integrity issues. Optical interconnect networks based on silicon photonic devices can potentially offer ultra-high bandwidth, low power, and low latency to address in-rack, inter-chip, and intra-chip communication challenges. Silicon-based photonic devices, such as optical waveguides and microresonators, have been demonstrated in CMOS-compatible fabrication processes and can be used to build low-cost inter/intra-chip optical networks. This talk will discuss the opportunities and challenges of this emerging technology and present our recent findings.

**15:00-15:30**    **Break**

**15:30-17:00**    **Special Invited Lecture 2**  
*Chair: Tohru Ishihara (Kyoto Univ.)*

15:30-17:00    **Architectural Approaches to using STT-RAM for Low-Power Caches**  
*Kiyoung Choi (Seoul National Univ., Korea)*

**Abstract:** Spin-Transfer Torque RAM (STT-RAM), a non-volatile magnetoresistive memory, is getting much attention these days due to its excellent characteristics. In particular, there are attempts to use it for on-chip caches since it is fast enough, scalable, and easily integrated into a CMOS chip. This talk presents various architectural approaches to using STT-RAM for on-chip caches. In particular, it presents various techniques to alleviate the overhead in writing data into the STT-RAM and thus reduce power consumption without degrading the system performance. The approaches target instruction caches, data caches, as well as unified last-level caches in single core or multi-core architectures.

**April 21, 2016 Main Hall(7th Floor), Yokohama Joho Bunka Center**  
**(Yokohama Media & Communications Center)**

**9:30-9:50      Session I**

**9:30-9:50      Welcome and Opening Remarks**

*Chair: Yuki Kobayashi (NEC)*

*Hiroaki Kobayashi,      Chair of the Organizing Committee*

*Allen J. Baum              Chair of IEEE/CS TCMM*

*Minoru Fujishima        Chair of IEICE/ICD TC*

**9:50-10:40    Session II**

9:50-10:40    **Keynote Presentation 1**

*Co-chairs: Hideharu Amano (Keio Univ.), Kunio Uchiyama (Hitachi)*

**Sub-pj per Operation Scalable Computing – the Next Challenge**

*Luca Benini (ETHZ, Switzerland)*

**Abstract:** The “internet of everything” envisions trillions of connected objects loaded with high-bandwidth sensors requiring massive amounts of local signal processing, fusion, pattern extraction and classification. From the computational viewpoint, the challenge is formidable and can be addressed only by pushing computing fabrics toward massive parallelism and brain-like energy efficiency levels. CMOS technology can still take us a long way toward this vision. Our recent results with the PULP (parallel ultra-low power) open computing platform demonstrate that pj/OP (GOPS/mW) computational efficiency is within reach in today’s 28nm CMOS FDSOI technology. In this talk, I will look at the next 1000x of energy efficiency improvement, which will require heterogeneous 3D integration, mixed-signal, approximate processing and non-Von-Neumann architectures for scalable acceleration.

**10:40-11:30    Session III**

10:40-11:30    **Keynote Presentation 2**

*Co-chairs: Yuki Kobayashi (NEC), Masato Suzuki (Socionext)*

**Power Optimization Leveraging FPGA and Voltage Regulator Chip Co-Design**

*Ashraf Lotfi (Intel, USA)*

**Abstract:** This talk will discuss areas of power savings that can be attained by considering the design of a voltage regulator (VR) concurrently with its FPGA loads. By knowing the power state of an FPGA in time and temperature one can communicate vital information to specially designed VRs where degrees of freedom can be leveraged to reduce the total power consumption seen by the power source driving the point-of-load VR delivering power to the FPGA. Areas of optimization and co-design include: (a) VR design techniques such as VR accuracy, reduction of IR drop and splitting VRs into smaller sections that can also act as power gates; or (b) VR control algorithm techniques that allow for computation of optimum operating points, particularly at full power and high temperature states as well as possibilities for future implementation of dynamic power savings.

**11:30-11:40    Break**

- 11:40-12:10**     **Session IV: Poster Short Speeches**  
*Chair: Koji Hashimoto (Fukuoka Univ.)*
- Poster 1     **Fast and Simple Netlist-level Fault-Injection Framework on FPGA**  
*Kazuki Zenba<sup>1</sup>, Tanvir Ahmed<sup>1</sup>, and Yuko Hara-Azumi<sup>1,2</sup> (<sup>1</sup>Tokyo Institute of Technology, <sup>2</sup>JST PRESTO)*
- Poster 2     **Prototyping Secure Process Virtual Machine Implementation with NanoBridge-based FPGA**  
*Qian Zhao<sup>1</sup>, Yukikazu Nakamoto<sup>1</sup> and Yukihide Tsuji<sup>2</sup> (<sup>1</sup>Univ. of Hyogo, <sup>2</sup>NEC)*
- Poster 3     **A Preliminary Study on Fine-Grained Heterogeneous Clustered Core**  
*Anri SUZUKI<sup>1</sup>, Ikumi KANEKO<sup>1</sup>, Ryotaro KOBAYASHI<sup>1</sup>, Hajime SHIMADA<sup>2</sup> (<sup>1</sup>Toyohashi Univ. of Technology, <sup>2</sup>Nagoya Univ.)*
- Poster 4     **Application-Aware DFS for Real-time Systems**  
*An Hsia, Ching-Wen Chen, and Yu-Xiang Wang (Feng Chia Univ.)*
- Poster 5     **Safe Microcontroller with On-Chip Bus Transition Monitor and Glitch-Free Backup Clock Changer for Clock-Failure Protection**  
*Joonghyun An, Jeonghun Cho, and Daejin Park (Kyungpook National Univ.)*
- Poster 6     **Leakage Power Optimization of a coarse grained reconfigurable accelerator by middle-grained body bias control**  
*Yusuke Matsushita, Hayate Okuhara, Koichiro Masuyama, Yu Fujita, and Hideharu Amano (Keio Univ.)*
- Poster 7     **Reducing leakage power of TLB by body biasing of the SOTB**  
*Daiki Kawase, Hayate Okuhara, and Hideharu Amano (Keio Univ.)*
- Poster 8     **x-Folded TM Architecture - A Folded Scheme Implementation in Interconnection Networks**  
*Mehrnaz Moudi, Mohamed Othman, Kweh Yeah Lun, and Amir Rizaan Abdul Rahiman (Univ. Putra Malaysia)*
- Poster 9     **Low Power Pre-encoded Radix-4 Booth Multiplier**  
*Yu-Cheng Cheng, Shao-Chi Liao, Tung-Chi Wu, and Yen-Jen Chang (National Chung Hsing Univ.)*
- Poster 10     **An Effective Lossless Embedded Compressor for UHD**  
*Jaesin Lee, Imjae Hwang, Minji Lee, Dukki Hong, and Woo-Chan Park (Sejong Univ.)*
- Poster 11     **A Case Study on Exploration of FPGA-based Multicore/Manycore Architectures**  
*Muneyuki Takenae, Itetsu Taniguchi, and Hiroyuki Tomiyama (Ritsumeikan Univ.)*
- Poster 12     **Feasibility Study of on-Chip Adaptive Body-bias for Ultra Low-power NoC Systems**  
*Akram Ben Ahmed, Hayate Okuhara, and Hideharu Amano (Keio Univ.)*
- Poster 13     **Audio Down-Mixing Hardware Based on Sound-tracing**  
*Dukki Hong, Hyuck-Joo Kwon, Juwon Yun, and Woo-Chan Park (Sejong Univ.)*
- Poster 14     **On-the-fly data compression for ExpEther NIC**  
*Hideki Shimura, Takuji Mitsuishi, and Hideharu Amano (Keio Univ.)*

- Poster 15 **Energy-saving Control based on Dynamic Prediction with Exponential Smoothing on KVM Virtualized Environments**  
*Atsushi Koshiba, Linzhan Guo, Mikiko Sato, and Mitaro Namiki (Tokyo Univ. of Agriculture and Technology)*
- Poster 16 **Construction of an environment for satellite engine simulation with Zynq**  
*Ryotaro Sakai<sup>1</sup>, Takaaki Miyajima<sup>2</sup>, Naru Sugimoto<sup>1</sup>, Naoyuki Fujita<sup>2</sup>, and Hideharu Amano<sup>1</sup> (<sup>1</sup>Keio Univ., <sup>2</sup>JAXA)*
- Poster 17 **Performance and Power Evaluation of FPGA-based Tsunami Simulator using Floating-Point DSPs**  
*Kohei Nagasu<sup>1</sup>, Kentaro Sano<sup>1</sup>, Fumiya Kono<sup>2</sup>, and Naohito Nakasato<sup>2</sup> (<sup>1</sup>Tohoku Univ., <sup>2</sup>Univ. of Aizu)*
- Poster 18 **Pipelining a Large Combinational Array in CC-SOTB as a Coarse Grained Reconfigurable Architecture**  
*Naoki Ando, Koichiro Masuyama, Yu Fujita, Hayate Okuhara, and Hideharu Amano (Keio Univ.)*
- Poster 19 **A 20uA/MHz at 200MHz Microcontroller with Low Power Memory Access Scheme for Small Sensing Nodes**  
*Masami Nakajima and Ichiro Naka (Renesas Electronics)*
- Poster 20 **Ultra low-complex IEEE 802.11ah Viterbi Decoder for IoT Applications**  
*Hirosasa Kato, Thi Hong Tran, and Yasuhiko Nakashima (Nara Institute of Science and Technology)*
- Poster 21 **Performance Improvement of FPGA-Based Stream Computing by Bandwidth Compressor**  
*Tomohiro Ueno, Kentaro Sano, and Satoru Yamamoto (Tohoku Univ.)*
- Poster 22 **Enhancing Performance of NUCA by Bank Sharing Mechanism**  
*Kuei-Chung Chang, Chin-Sheng Yu, and Yang-Ching Su (FengChia Univ.)*
- Poster 23 **Stream-based FPGA implementation of a particle filter for real-time image processing**  
*Akane Tahara, Yoshiki Hayashida, Yuichiro Shibata, and Kiyoshi Oguri (Nagasaki Univ.)*
- Poster 24 **A Power-Performance Tradeoff of HBM by Limiting Access Channels**  
*Takuya Toyoshima, Masayuki Sato, Ryusuke Egawa, and Hiroaki Kobayashi (Tohoku Univ.)*
- Poster 25 **An efficient FPGA implementation of co-occurrence feature calculation in FIND features**  
*Yoshiki Hayashida, Masahito Oishi, Ryo Fujita, Yuichiro Shibata, and Kiyoshi Oguri (Nagasaki Univ.)*
- Poster 26 **Hardware Architecture for Online Frequent Itemset Mining with Memory-Efficient Data Structure**  
*Kasho Yamamoto, Tetsuya Asai, and Masato Motomura (Hokkaido Univ.)*
- 12:10-13:10 Lunch Time Break**
- 13:10-14:10 Poster Open: 7th floor poster show room**
- 14:10-15:00 Session V**

14:10-15:00

**Keynote Presentation 3**

*Co-chairs: Akihiko Hashiguchi (Sony), Yoshio Hirose (Fujitsu Labs.)*

**Modality of CMOS Image Sensor Competition**

*Teruo Hirayama (Sony)*

**Abstract:** The CMOS image sensor is currently dominant on the image sensor market. However, until the early 2000s, CCD was mainly used in video cameras and digital still cameras, because its image quality was superior to that of the CMOS image sensor. Through development of improved technology and utilization of its benefits including original high-speed, low power consumption, and digital output, the CMOS image sensor has been widely used in smart phones and replaced CCD as the main image sensor on the market in the late 2000s. In addition to video cameras, digital still cameras, and smartphones, use of CMOS image sensor has spread to such areas as security-monitoring, in-vehicles, and medical. In these fields, it needs to utilize photon information such as infrared light, distance, polarization, etc., which have not been used very much for video cameras or digital still cameras. I will describe the key points to expand the image sensor market, including how the CMOS image sensor replaced CCD.

15:00-15:50

**Session VI**

15:00-15:50

**Keynote Presentation 4**

*Co-chairs: Yasuo Unekawa (Toshiba), Chikafumi Takahashi (Renesas System Design)*

**The Multiscale Dataflow Computing Chip**

*Oskar Mencer (Imperial College London and Maxeler Technologies, UK)*

**Abstract:** Multiscale Dataflow Computing consists of a core architecture as well as a design process for splitting computing into a control-plane and data-plane, similar to software defined networking[1]. Currently, Maxeler's dataflow computers are running on top of large amounts of DRAM connected via FPGA chips, yielding a 20-50x speed advantage[2] over top end microprocessors. To achieve a further 10-20x in performance, Maxeler is designing a Dataflow computing chip capable of maximizing performance per cubic foot of datacenter space as well as maximizing performance per Watt (and performance per power supply). Over the years, Maxeler has shown a wide range of applications running very efficiently on dataflow computers, such as Seismic Imaging, Monte Carlo simulations, video encoding, Quantum Chromodynamics, (financial) transaction processing, SNORT, climate modelling, CFD, and machine learning. The vast infrastructure and collection of applications will form the basis for deployment in the Cloud as well as a justification to build a completely new kind of computing device. For a gallery of applications see <http://appgallery.maxeler.com>

15:50-16:05

**Break (Poster Open: 7th floor poster show room)**

16:05-17:20

**Session VII: Recognition**

*Chair: Takuya Azumi (Osaka Univ.)*

16:05-16:30

**193 MOPS/mW @ 162 MOPS, 0.32V to 1.15V Voltage Range Multi-Core Accelerator for Energy-Efficient Parallel and Sequential Digital Processing**

Davide Rossi<sup>1</sup>, Antonio Pullini<sup>2</sup>, Igor Loi<sup>1</sup>, Michael Gautschi<sup>2</sup>, Frank Kagan Gurkaynak<sup>2</sup>, Adam Teman<sup>3,4</sup>, Jeremy Constantin<sup>3</sup>, Andres Burg<sup>3</sup>, Ivan Miro-Panades<sup>5</sup>, Edith Beigne<sup>5</sup>, Fabien Clermidy<sup>5</sup>, Fady Abouzeid<sup>6</sup>, Philippe Flatresse<sup>6</sup>, and Luca Benini<sup>1</sup> (<sup>1</sup>Univ. of Bologna, <sup>2</sup>ETH Zurich, <sup>3</sup>EPFL, <sup>4</sup>Bar-Ilan Univ., <sup>5</sup>CEA

LETI, <sup>6</sup>ST Microelectronics)

**16:30-16:55**    **A 1.1mW 32-thread Artificial Intelligence Processor with 3-level Transposition Table and On-chip PVT Compensation for Autonomous Mobile Robots**  
*Youchang Kim, Dongjoo Shin, Jinsu Lee, and Hoi-Jun Yoo (KAIST)*

**16:55-17:20**    **An Energy-Efficient Parallel Multi-Core ADAS Processor with Robust Visual Attention and Workload-Prediction DVFS for Real-Time HD Stereo Stream**  
*Kyuho Lee, Kyeongryeol Bong, Changhyeon Kim, Junyoung Park, and Hoi-Jun Yoo (KAIST)*

**17:20-17:30**    **Break**

**17:30-19:00**    **Session VIII: Panel Discussions**

**Topics: “Computing and Communication Evolution for IoT Innovations”**

*Organizer & Moderator: Hiroaki Nishi (Keio Univ.)*

*Panelists: Jiang Xu (Hong Kong Univ. of Science and Technology, China)*

*Luca Benini (ETHZ, Switzerland)*

*Michael McCool (Intel, USA)*

*Toshitsugu Sakamoto (NEC)*

*Shingo Fujimoto (Fujitsu)*

**April 22, 2016 Main Hall(7th Floor), Yokohama Joho Bunka Center**  
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**9:30-10:20      Session IX**

9:30-10:20      **Keynote Presentation 5**

*Co-chairs: Koyo Nitta (NTT Electronics), Ryusuke Egawa (Tohoku Univ.)*

**New Frontiers in Computing**

*Michael McCool (Intel, USA)*

**Abstract:** Recently some exciting changes have taken place in computing. I will be presenting an update on Intel's involvement in these developments. First, powerful many-core graphics accelerators continue to be integrated into Intel desktop and mobile processors. The latest Gen 9 graphics cores in Intel's 6th generation (Skylake) processors have some interesting new capabilities, especially around their ability to share data with the CPU cores on the same chip. Their performance is also scaling extremely rapidly with each generation, so much so that they have become interesting targets for non-graphics computations. Secondly, Intel recently closed an acquisition of Altera. Altera FPGAs bring a set of new opportunities in computing with are complementary to Intel's traditional strengths. FPGAs can and are being used for acceleration, but also have unique capabilities to support hard real-time computing and flexible hardware interfaces. They are also capable of accelerating computations at lower power levels than alternative approaches. The key challenge with FPGAs is making the programming model approachable to traditional software developers. Third, Intel's Xeon Phi architecture continues to evolve and find new applications. I will survey some of the opportunities and issues with this architecture. Massively parallel and vectorised programming is the key to taking advantage of the Intel Xeon Phi architecture. I will review some of the parallel programming models that have developed for it. Fourth, Intel has been pushing down further into low power, lightweight processors to enable the Internet of Things, but there are many challenges to be overcome in the programming model before the IoT can reach its full potential. Fifth, I will talk about the requirements for an emerging new class of computing platforms: robots. Finally, to wrap up, I will discuss neuromorphic computing and its potential for dramatically transforming computing.

**10:20-10:40      Break (Poster Open: 7th floor poster show room)**

**10:40-11:20      Session X: Memory**

*Co-chairs: Hajime Shimada (Nagoya Univ.), Hidetoshi Matsumura (Fujitsu Labs.)*

10:40-11:05      **A Cache Partitioning Mechanism to Protect Shared Data for CMPs**

*Masayuki Sato, Shin Nishimura, Ryusuke Egawa, Hiroyuki Takizawa, and Hiroaki Kobayashi (Tohoku Univ.)*

11:05-11:20      **Powering-off DRAM with Aggressive Page-out to Storage-class Memory in Low Power Virtual Memory System**

*Yusuke Shiota, Shiyo Yoshimura, Satoshi Shirai, and Tatsunori Kanai (Toshiba)*

**11:20-11:40      Break (Poster Open: 7th floor poster show room)**

**11:40-12:45      Session XI: Low Power Processing**

*Co-chairs: Shintaro Izumi (Kobe Univ.), Kotaro Shimamura (Hitachi)*

- 11:40-12:05 **MuCCRA4-BB: A Fine-Grained Body Biasing Capable DRP**  
*Johannes Maximilian Kühn<sup>1,2</sup>, Akram Ben Ahmed<sup>2</sup>, Hayate Okuhara<sup>2</sup>, Hideharu Amano<sup>2</sup>, Oliver Bringmann<sup>1</sup>, and Wolfgang Rosenstiel<sup>1</sup> (<sup>1</sup>Univ. of Tübingen, <sup>2</sup>Keio Univ.)*
- 12:05-12:30 **A 20uA/MHz at 200MHz Microcontroller with Low Power Memory Access Scheme for Small Sensing Nodes**  
*Masami Nakajima, Ichiro Naka, Fumihiko Matsushima, and Tadaaki Yamauchi (Renesas Electronics)*
- 12:30-12:45 **ASIC Design of MUL-RED Radix-2 Pipeline FFT Circuit for 802.11ah System**  
*Thi Hong Tran, Soichiro Kanagawa, Duc Phuc Nguyen, and Yasuhiko Nakashima (Nara Institute of Science and Technology)*
- 12:45-13:55 Lunch Time Break**
- 13:55-14:35 Session XII**
- 13:55-14:35 **Invited Presentation 1**  
*Co-chairs: Yukinori Sato (Tokyo Tech.), Yuki Kobayashi (NEC)*
- NanoBridge-based FPGA in Harsh Environments**  
*Makoto Miyamura (NEC)*
- Abstract:** High-temperature operations are essential in harsh environments for the control units of robot, automobile, spacecraft and so on. Further advancement of computing power for the accurate control of these apparatus is also an increasing demand. As a solution for such applications, specific microcontrollers have been adopted. They offer a good programmability and high reliability, but in turn, it has a limited performance in real-time and low-power processing. We have developed a novel non-volatile and small-footprint switching element, called NanoBridge (NB). The NB is a via-like (i.e., inter-metal layer) switching element with low capacitance. Due to its endurance against high temperature, noise, and radiation, NB-based FPGA is suitable for the control units in harsh environments. The advantage of the low-voltage and intermittent operation also allow NB-FPGA to be used as power efficient off-loader for widely spreading IoT devices.
- 14:35-14:45 Break (Poster Open: 7th floor poster show room)**
- 14:45-15:50 Session XIII: FPGA and Software**  
*Co-chairs: Yasutaka Wada (Meisei Univ.), Hiroyuki Takizawa (Tohoku Univ.)*
- 14:45-15:00 **How SIMD Width Affects Energy Efficiency: A Case Study on Sorting**  
*Hiroshi Inoue (IBM Research - Tokyo)*
- 15:00-15:25 **Thermal safety through limp home mode for intelligent rear view camera systems**  
*Piyali Goswami<sup>1</sup>, Yogesh Marathe<sup>1</sup>, Kedar Chitnis<sup>1</sup> and Koichi Saito<sup>2</sup> (<sup>1</sup>ADAS Software, <sup>2</sup>Texas Instruments)*
- 15:25-15:50 **A Power-efficient FPGA Accelerator: Systolic Array with cache-coherent interface for Pair-HMM Algorithm**  
*Megumi Ito, and Moriyoshi Ohara (IBM Research - Tokyo)*
- 15:50-16:10 Break (Poster Open: 7th floor poster show room)**
- 16:10-17:00 Session XIV**



16:10-17:00

**Keynote Presentation 6**

*Co-chairs: Ryusuke Egawa (Tohoku Univ.), Koyo Nitta (NTT Electronics)*

**Cool Techniques for Hot Chips**

*Mateo Valero (Barcelona Supercomputing Center, Spain)*

**Abstract:** Some decades ago, computer architecture techniques were focused on maximizing performance by means of exploiting Instruction Level Parallelism (pipelining, VLIW, superscalar or out-of-order execution) or Data Level Parallelism (vector instructions). Power efficiency was not the main priority in those designs, although some of these techniques demonstrated a lot of potential in terms of energy efficiency. Nowadays, the situation has dramatically changed: maximizing the performance per energy ratio is as important as increasing performance itself. In this talk, we will revisit some computer architecture ideas and explain how are they being used in the context of the RoMoL project, which proposes the concept of Runtime-Aware Architecture (RAA) as its fundamental contribution. In RAA's the parallel runtime layer drives the design of new hardware components, which leads to increased performance and reduced power consumption.

17:00-17:20

**Poster Award and Closing Remark**

*Makoto Ikeda, Program Committee Co-chair (Univ. of Tokyo)*