

Final Program

April 18, 2007 Main Hall(7th Floor), Yokohama Joho Bunka Center
(Yokohama Media & Communications Center)

13:00-15:30 Special Session 1

Chair: Koji Inoue (Kyushu University)

13:00-15:30 Novel Architectural Techniques to Mitigate Processor Errors due to Design Defects and Parameter Variation

Speaker: Josep Torrellas (University of Illinois, Urbana-Champaign, U.S.A.)

Abstract:

As feature size decreases and more transistors are integrated on a chip, processor designers face mounting challenges. Perhaps two of the most formidable ones are verifying the increasingly complex designs and dealing with parameter variation cost-effectively. In this talk, I will describe some novel architectural techniques to address these challenges.

To deal with increased design complexity and the resulting design errors, we propose Phoenix. Phoenix is on-chip field-programmable hardware that taps key logic signals and, based on downloaded error signatures, combines the signals into conditions that flag design errors. On error detection, Phoenix attempts to recover. With the Phoenix hardware, hardware design errors can be treated like system software bugs, with vendors periodically releasing patches that fix hardware in the field.

Parameter variation affects processor pipelines by making some pipeline stages slower and others faster. The result is a slower processor, since a pipeline must be clocked at the frequency of its slowest stage. To improve performance, we propose ReCycle, a technique where the pipeline is clocked with the average frequency of all the pipeline stages. This is accomplished by skewing pipeline latches after fabrication to redistribute the timing slack within pipeline loops. We further strategically inject slack into critical pipeline loops, which ReCycle can then leverage.

15:30-16:00 Break

16:00-18:30 Special Session 2

Chair: Koji Inoue (Kyushu University)

16:00-18:30 Architectural Integration of Software Protection

Speaker: Gyungho Lee (University of Illinois, Chicago, U.S.A.)

Abstract:

Software protection has been the focus of numerous academic research and commercial development efforts. Many protection schemes have been proposed to make it difficult to analyze and tamper program behavior. However, the majority of software attacks are based on exploits that alter program behavior at run time such as buffer overflow, format string, and integer overflow. Such exploits remain often untouched even after preventive measures done by the protection schemes. Also, software tools or patches, either removing or detecting known exploits, have been utilized but with limited success because they cannot deal with new types of attacks. Several intrusion detection schemes have been developed to provide

protection from yet-unknown new types of attacks but with limited deployment due to high overhead and ineffectiveness. The control flow altering exploits are possible due to a semantic gap in program description and its execution: the program behavior described in software may not be the one carried out by machine architecture because control flow tracking at machine instruction level is blindfolded without a validity check in the current processor architecture. Whenever this semantic gap is not properly handled at a higher level by system and application software, it becomes a vulnerability that malicious attacks exploit. Along with a review of technical issues and proposed schemes in software protection, which suggests infeasibility of filling the gap by software alone, this talk introduces an architectural approach for enforcing legitimate control flow tracking at the machine instruction level to fill the semantic gap.

April 19, 2007 Main Hall(7th Floor), Yokohama Joho Bunka Center
(Yokohama Media & Communications Center)

9:30-9:50 Session I

9:30-9:50 **Welcome and Opening Remarks**

Chair: Kazumasa Suzuki (NEC)

Tadao Nakamura

Chair of the Organizing Committee

Josep Torrellas

Chair of TCCA, The IEEE Computer Society

Ryoichi Tsukahara

*Director General of Economic Affairs Bureau,
Yokohama City*

9:50-10:40 **Keynote Presentation 1**

Chair: Hajime Kubosawa (Fujitsu Labs.)

The Next Generation Supercomputer Project and Its Technical Issues

Tadashi Watanabe (RIKEN)

The Japanese government has selected the supercomputing technology as one of the key technologies in “The Third Science and Technology Basic Plan” which is a five-year plan started in the fiscal year of 2006. The MEXT (Japanese Ministry of Education, Culture, Sports, Science and Technology) has started the “Development and Application of the Next Generation Supercomputer Project” in 2006 based on this governmental basic plan. RIKEN was assigned as the project headquarters to promote this project and develop a world-fastest supercomputer and related application software.

In this project, the following academic-industrial collaborative activities are conducted under the initiative of MEXT.

- Development and implementation of a 10 PFLOPS class advanced high-performance supercomputer.
- Development and dissemination of application software that makes optimum use of the supercomputer.
- Establishment of the advanced and highest standard supercomputing Center of Excellence (COE) equipped with the Next Generation Supercomputer for a principal computing resource.

In this project, we develop not only the supercomputer but also grid middleware called the NAREGI program to utilize distributed computer resources through the nationwide high-speed network called the Cyber Science Infrastructure. Furthermore, the supercomputer will be developed and widely used in general-purpose technical applications such as fluid dynamics, structural analysis, climate modeling, fusion science and astrophysics. Especially, we expect that the application software system developed for nano- and life-science will bring major breakthroughs to science and technology.

The current schedule of the project is as follows. A part of the system will be completed at the end of the fiscal year of 2010 and start to operate right after the installation. The whole system will be completed by the end of March in 2012 with sustained performance of over PFLOPS in several applications of the above mentioned technical computing subjects.

At the beginning of 2006, we started a conceptual design process to define system architecture for the next supercomputer system. To select important software for the system, the application study committee was formed in January 2006. The committee has selected 21 applications. The selected software covers the important technical computing subjects of nano-science, life-science, geophysics, physics, astrophysics, and engineering. We are currently studying and evaluating several

system architectures proposed by industries and universities to attain sustained performance of over PFLOPS in these selected applications.

The whole scope of the project including critical technical issues and the project schedule will be presented at this talk.

10:40-11:00 Break

11:00-11:40 Session II

Chair: Michinori Nishihara (IBM)

11:00-11:40

Invited Presentation 1

A 65nm SPE for a 1 Petaflop Super Computer

Brian Flachs (IBM, U.S.A.)

This presentation discusses the application of the Cell Broadband Engine to the field of high performance computing. The importance of heterogeneous processing and high design frequency to power limited applications is presented with an introduction to the Cell Architecture. The effectiveness of the CBE concept is demonstrated by some performance data. A new CBE implementation for HPC called the Enhanced Broadband Engine is introduced. Its application within a peta-flop class super computer based upon the Enhanced Broadband Engine is discussed.

11:40-13:00 Sponsored Lunch (Royal Hall Yokohama)

"Platform-Based Design with MIPS"

Realizing the benefits of best-in-class IP and ESL Alliances

(MIPS Technologies)

13:00-13:50 Session III: High-performance Computing

Chair: Yuetsu Kodama (AIST)

13:00-13:25

System Wide Software Development Tools for Heterogeneous Programming, Debug and Profiling of Mixed Multi-core and Acceleration Processors (PC invited Paper)

Ray McConnell (ClearSpeed Technology Plc., U.K.)

13:25-13:50

Power-Performance Evaluation on Ultra-Low Power High-performance Cluster System : MegaProto/E

Takayuki Imada, Mitsushiba Sato, Yoshihiko Hotta, Hideaki Kimura, Taisuke Boku, Daisuke Takahashi, Shin'ichi Miura, and Hiroshi Nakashima (University of Tsukuba / Kyoto University)

13:50-14:15 Session IV: Poster Short Speeches

Chair: Toshinori Sato (Kyusyu University)

Poster 1 **An Automatic Level Control ASK Modulator for UHF-band RFID Applications**

Kyu-Sung Chae, Chang-Woo Kim (Kyung Hee University, Korea)

Poster 2 **XNoTs: Crossbar-Connected Multi-Layer Topologies for 3-D NoCs**

Hiroki Matsutani (Keio University), Michihiro Koibuchi (National Institute of Informatics), Hidenori Amano (Keio University)

Poster 3 **Low Power NoC Design for tiled CMP Using Zero-Efficient Scheme**

Kun Huang, Jun Wang, Ge Zhang (Chinese Academy of Sciences, China)

Poster 4 **A Multi-Performance Processor for Low Power Embedded Applications**

Yuichiro Oyama, Tohru Ishihara, Toshinori Sato, Hiroto Yauura (Kyushu University)

- Poster 5 **A Fair-Sharing and Power-Aware L2 Cache System for Chip Multiprocessors**
Isao Kotera, Hiroyuki Takizawa, Hiroaki Kobayashi (Tohoku University)
- Poster 6 **Transmission Combining Arbiter for Multiple ROP Units in 3D Graphics Accelerators**
Il-San Kim, Jae-Ho Nah, Tack-Don Han (Yonsei University, Korea)
- Poster 7 **A Framework for Real Time Ray Tracing**
Kyungho Lee (Sejong University, Korea), Sangduk Kim, Jaeho Nah, Yoon-Sig Kang (Yonsei University, Korea), Dongseok Kim (Sejong University, Korea), Sang-Won Ha, Sung-Bong Yang, Tack-Don Han (Yonsei University, Korea), Woo-Chan Park (Sejong University, Korea)
- Poster 8 **A Low-Power Embedded Processor with Java Hardware Interpreter**
Jong-Sung Lee, Hyeong-Cheol Oh (Korea University, Korea)
- Poster 9 **Reverse Engineering on the Processor with Program Protection Feature**
Junichi Yamashita, Takekazu Tabata, Toshiaki Kitamura (Hiroshima City University)
- Poster 10 **Power Reduction Technique for Dynamically Reconfigurable Processor**
Takashi Nishimura, Keiichiro Hirai (Keio University), Seidai Takeda (Shibaura Institute of Technology), Yohei Haswgawa, Satoshi Tutumi, Hedeharu Amano (Keio University), Kimiyoshi Usami (Shibaura Institute of Technology)
- Poster 11 **Power Consumption Reduction Method of Dynamic Optically Reconfigurable Gate Array VLSIs**
Minoru Watanabe, Fuminori Kobayashi (Kyushu Institute of Technology)
- Poster 12 **P3 - Performance and Power Optimization Tool for Portable Embedded Systems**
Yasuteru Kohda, Kohji Takano, Gang Zhang, Nobuyuki Ohba (IBM)
- Poster 13 **Compiler Design Techniques for Efficiently Translating Radio Protocol Description Machine Language to Hybrid Asynchronous ISA**
Dipnarayan Guha, Thambipillai Srikanthan (Nanyang Technological University, Singapore)
- 14:15-14:55 Break** (Poster Open: 7th floor poster show room)
- 14:55-16:30 Session V: Low-Power Cache and Circuits**
Chair: Hiroaki Suzuki (Renesas Technology)
- 14:55-15:10 **Delay Sensitivity Study on Process, Supply Voltage and Temperature Variations of Single Edge-Triggered Flip-Flops**
W.L.Goh, K. S. Yeo, and M.W.Phyu (Nanyang Technological University, Singapore)
- 15:10-15:25 **Low Static Powered Asynchronous Data Transfers Based on Current-Mode Multiple Valued Logic for GALS Systems**
Myeong-Hoon Oh and Seong-Woon Kim (Electronics and Telecommunications Research Institute, Korea)
- 15:25-15:50 **Dynamic Management Technique to Mitigate Performance Degradation for Low-Leakage Caches**

Reiko Komiya, Koji Inoue, and Kazuaki Murakami (Kyushu University)

- 15:50-16:05 **Fast Way-predicting Instruction Cache for Energy Efficiency and High Performance**
Cuiping Xu and Ge Zhang (Institute of Computing Technology, Chinese Academy of Science, China)
- 16:05-16:30 **Reduce leakage and dynamic energy in I-Cache with two-port way predictor**
Zhou Hongwei, Zhang Chengyi, Zhang Minxuan, and Xing Zuocheng (National University of Defense Technology, China)
- 16:30-16:50 **Break** (Poster Open: 7th floor poster show room)
- 16:50-18:50 **Session VI: Panel Discussions**
Microprocessor for 10-Peta FLOPS Supercomputer
Organizer & Moderator: Ryutaro Himeno (RIKEN)
Panelists: TBD
- 19:00-21:00 **Banquet** (Hotel Monterey Yokohama)
Chair: Yoshiaki Hagiwara (Sony)

April 20, 2007 Main Hall(7th Floor), Yokohama Joho Bunka Center
(Yokohama Media & Communications Center)

9:30-10:20 Session VII
Chair: Yasuo Unekawa (Toshiba)

9:30-10:20 **Keynote Presentation 2**
Toshiba's Strategy in Semiconductor Business and NAND Flash Memory
Shozo Saito (Toshiba)

Toshiba semiconductor business is rapidly recovered and returned to higher profit and stable business. We aim to achieve more profitable growth and to be in world wide No.3 position by increasing sales revenue over the market growth rate. In order to achieve this goal, Toshiba focus on five strategic products like NAND Flash memory, MCP for mobile phone, system LSI and discrete device.

Strategy on NAND Flash memory are expanding capacity with 300mm wafer fabrication plant and creating new application markets such as MP3 audio player, imaging application, mobile phone and memory cards. We are also developing cutting-edge process technology for next three generation simultaneously, 56nm, 4Xnm and 3Xnm, and to sustain competitive advantage like a production efficiency, cost and IP.

We would like to explain our business plan and strategy of semiconductor business and NAND flash memory. We also show you NAND Flash memory market demand and our product line-up and capacity. Finally, we discuss our technology roadmap of Logic and memory devices, and future memory technology not only NAND Flash memory but also nonvolatile RAM etc.

10:20-11:00 Session VIII
Chair: Yusuke Nitta (Renesas Technology)

10:20-11:00 **Invited Presentation 2**
EXREAL Platform : SOC Design Challenges for Embedded Systems
Toshihiro Hattori (Renesas Technology)

“System On Chip” can realize very complex embedded systems, such as, mobile phones with multi-media functions. These embedded systems require not only very complex SOC’s but also very huge software. The important design targets like performance, low-power, cost, and time-to-market should be evaluated in system level. For example, one of the most important design targets in SOC design is to reduce the software design cost. And system performance should be optimized as a combination of huge software and complex SOC’s.

Platform design approach is one of the solutions of these new challenges in embedded system design. Standardizations can allow the reuse of design but restrict the flexibility of the embedded systems. The integrated embedded systems require the “divergence” to application specific solutions. On the other hand, many common functions are implemented in different application areas. This means the “convergence” is also important in the current embedded systems.

In this speech, I will show the concept of “EXREAL Platform” which is mother platform to establish the application specific platforms. EXREAL Platform connects not only hardware IP but also software IP and also enables optimization of systems.

11:00-11:30 Break (Poster Open: 7th floor poster show room)

- 11:30-12:20** **Session IX: Special Applications**
Chair: Fumio Arakawa (Hitachi)
- 11:30-11:55 **Indirect Branch Validation Unit for Secure Program Execution**
Y.Shi, A.Lee, G.Lee, T-J Park, T-C Jung, and B-C Kang (University of Illinois, U.S.A.)
- 11:55-12:20 **Toward Ubiquitous Biomedical Implantable Computing Chips - An Energy-Efficient Low-Power Architecture**
Allen C. Cheng (University of Pittsburgh, U.S.A.)
- 12:20-14:00** **Lunch Time Break**
- 14:00-14:40** **Session X: Video Codec**
Chair: Hideki Yamauchi (Samsung)
- 14:00-14:25 **An 880 mW full-spec HDTV MPEG-2 CODEC LSI for prosumer HDV camera with low-power adaptive search engine**
Yasuyuki Nakajima, Yutaka Tashiro, Hiroe Iwasaki, and Jiro Naganuma (NTT)
- 14:25-14:40 **Development of a Video Encoder for a Micro-capsule Robot**
Shingo Tomoda, Akihisa Furuhashi, Kaori Iida, Takayuki Murakami, Minoru Sakaida, Tomonori Izumi, and Hironori Yamauchi (Ritsumeikan University)
- 14:40-14:55** **Break** (Poster Open: 7th floor poster show room)
- 14:55-16:00** **Session XI: Media Processing**
Chair: Kiat Seng Yeo (Nanyang Tech. University, Singapore)
- 14:55-15:20 **A Wireless Audio/Video Network Processor Capable of HD-A/V Streaming Transmission with Contents Protection**
Tatsuo Shiozawa, Masanori Kuwahara, Toshio Fujisawa, Yukimasa Miyamoto, Masahiro Sekiya, Kouji Horisaki, Satoshi Kaburaki, Daisuke Taki, Keiko Shimizu, Hirotsugu Kajihara, Noriyasu Kato, Kiyotaka Matsue, Kuniaki Ito, Hiroyuki Hara, Ryouichi Bandai, Takeshi Miyaba, Shuuji Matsumoto, Keiko Seki-Fukuda, Yoshinori Watanabe, and Yasuo Unekawa (Toshiba / Toshiba Microelectronics)
- 15:20-15:45 **Implementation and Evaluation of the Processor for Stream Multimedia Applications using Dynamic Reconfiguration**
Yutaka Yamada, Takashi Yoshikawa, and Shigehiro Asano (Toshiba)
- 15:45-16:00 **A 2048-Point FFT Processor Based on Twiddle Factor Table Reduction**
Ji-Hoon Kim and In-Cheol Park (KAIST, Korea)
- 16:00-16:10** **Break**
- 16:10-17:50** **Session XII: Multicore**
Chair: Keiji Kimura (Waseda University)
- 16:10-16:35 **Power Saving Innovations in the P.A. Semi PA6T core**
Daniel Murray (P.A. Semi, U.S.A.)
- 16:35-17:00 **Automatic Parallelization for Speculative Multithreading Exposing Parallelism from Sub-structures of Programs by Graph Representation**
Masamichi Takagi, Taku Ohsawa, Shoji Kawahara, and Satoshi Matsushita (NEC / NEC Electronics)

- 17:00-17:25 **Scalable Multi-Core SoC Platform for Low-Powered Architecture**
Yukoh Matsumoto and Tadao Nakamura (TOPS Systems / Tohoku University)
- 17:25-17:50 **Resource Manager to Control Temperature for Embedded SOC**
Makoto Saen, Kenichi Osada, Satoshi Misaka, Tetsuya Yamada, Yoshitaka Tsujimoto, Yuki Kondoh, Tatsuya Kamei, Yutaka Yoshida, Ei Nagahama, Yusuke Nitta, Takayasu Ito, Tadashi Kameyama, and Naohiko Irie (Hitachi / Renesas Technology)
- 17:50-18:00 Closing Remarks**
Kunio Uchiyama, Program Committee Chair (Hitachi)