

Wed. 17

| Start | End | duration | Session | | "Title", Authors (Affiliations, Countries) | Chair | Co-Chair | TimeZone |
|-------|-------|----------|--|--|---|----------------------------|---------------------------|----------|
| 13:00 | 13:20 | 0:20 | Session I : Welcome & Opening Remarks | | | Y. Kobayashi (NEC) | H. Matsutani (Keio Univ.) | |
| 13:20 | 14:10 | 0:50 | Session II : Keynote Presentation 1 | Keynote | Accelerating AI with Analog In-Memory-Computing Stefano Ambrogio (IBM Research) | T. Ueda (IBM Japan) | H. Matsutani (Keio Univ.) | |
| 14:10 | 14:30 | 0:20 | Break | | | | | |
| 14:30 | 15:20 | 0:50 | Session III : Keynote Presentation 2 | Keynote | "Optical Neural Networks With In-Memory Computation and Tensor Decomposition" Stanley Cheung (Hewlett Packard Enterprise) | T. Ishihara (Nagoya Univ.) | H. Iwasaki (TUAT) | |
| 15:20 | 15:40 | 0:20 | Break | | | | | |
| 15:40 | 16:05 | 0:25 | Session IV : FPGAs and Reconfigurable Processors | | [14] Hoai Luan Pham, Hai Hau Nguyen, Vu Trung Duong Le, Tuan Hai Vu, Thi Diem Tran, Thi Hong Tran and Yasuhiko Nakashima, "MRCA: Multi-grained Reconfigurable Cryptographic Accelerator for Diverse Security" | | | |
| 16:05 | 16:20 | 0:15 | | [16] Takuya Kojima, Yosuke Yanai, Hayate Okuhara, Hideharu Amano, Morihiko Kuga and Masahiro Iida, "SLMLET: A RISC-V Processor SoC with Tightly-Coupled Area-Efficient eFPGA Blocks" | | | | |
| 16:20 | 16:35 | 0:15 | | [19] Zirui Lin, Kazuhiro Nakadai, Katsutoshi Itoyama and Hideharu Amano, "FPGA-based Low Power Acceleration of HARK Sound Source Localization" | | | | |
| 16:35 | 16:50 | 0:15 | | [34] Kento Mishima, Naoya Niwa, Kazutoshi Wakabayashi and Hiroe Iwasaki, "ISP Parameter Optimization and FPGA Implementation for Object Detection in Low-Light Conditions" | | | | |
| 16:50 | 17:00 | 0:10 | Break | | | | | |
| 17:00 | 17:40 | 0:40 | Special Invited Presentation | Invited presentation | "Achieving the most energy-efficient compute fabric for ML and HPC using of thousands of RISC-V cores" Dave Ditzel (Esperanto Technologies) | | | |

Thu. 18

| Start | End | duration | Session | Main Hall | Speaker | Chair | Co-Chair | TimeZone |
|-------|-------|----------|------------------------------------|--|--|-----------------------------------|---------------------|----------|
| 9:00 | 9:50 | 0:50 | Session V : Keynote Presentation 3 | Keynote | "Processing-in-Memory: from Technology to Products" Kyomin Sohn (Samsung Electronics) | Y. Sato (Toyoashi Univ. of Tech.) | Y. Hirose (Fujitsu) | |
| 9:50 | 10:10 | 0:20 | Break | | | | | |
| 10:10 | 10:35 | 0:25 | Session VI : SLAM Processors | | [24] Jueun Jung, Seungbin Kim, Bokyoung Seo, Wuyoung Jang, Sangho Lee, Jeongmin Shin, Donghyeon Han and Kyuho Lee, "A Low-power and Real-time Semantic LiDAR SLAM processor with Point Neural Network Segmentation and kNN Acceleration for Mobile Robots" | | | |
| 10:35 | 11:00 | 0:25 | | [25] Gwangtae Park, Seokchan Song, Haoyang Sang, Dongseok Im, Donghyeon Han, Sangyeob Kim, Hongseok Lee and Hoi-Jun Yoo, "A Low-power and Real-time Neural-Rendering Dense SLAM Processor with 3-Level Hierarchical Sparsity Exploitation" | | | | |
| 11:00 | 12:00 | 1:00 | Poster Session | | | | | |
| 12:00 | 13:00 | 1:00 | Lunch | | | | | |
| 13:00 | 14:30 | 1:30 | Special Invited Lecture 1 | | "Navigating Aging Realities: Integrating Reliability into Cutting-Edge Computing Systems" Yu-Guang Chen (National Central Univ. Taiwan) | J. Shiomi (Osaka Univ.) | | |
| 14:30 | 14:50 | 0:20 | Break | | | | | |
| 14:50 | 16:20 | 1:30 | Special Invited Lecture 2 | | "Radiation-hardened circuit design for space application" SinYoung Kim (imec) | J. Shiomi (Osaka Univ.) | | |
| 16:20 | 16:40 | 0:20 | Break | | | | | |
| 16:40 | 18:00 | 1:20 | Session VII : Panel Discussion | Panel | Exploring the Potential, Limits, and Challenges of PIM (Processing-in-Memory) and CIM (Computation-in-Memory) | Y. Nakashima (NAIST) | | |

Fri. 19

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|-------|-------|----------|---|--|---|------------------------|------------------------------|----------|
| 9:00 | 9:50 | 0:50 | Session VIII: Keynote Presentation 4 | Keynote | "Intel Foundry Advanced Packaging: enabling low-power client through AI and HPC" Peng Chunging (Intel) | T. Sakata (TIER IV) | R. Egawa (Tokyo Denki Univ.) | |
| 9:50 | 10:10 | 0:20 | Break | | | | | |
| 10:10 | 11:00 | 0:50 | Session IX : Keynote Presentation 5 | Keynote | "Hot AI by COOL SoCs" Hoi-Jun Yoo (KAIST) | Y. Kobayashi (NEC) | S. Sasaki (Toshiba) | |
| 11:00 | 11:20 | 0:20 | Break | | | | | |
| 11:20 | 11:45 | 0:25 | Session X : CNN and GCN | | [30] Seunghyun Park and Daejin Park, "Power-Efficient CNN Accelerator Design with Bit-Separable Radix-4 Booth Multiplier" | | | |
| 11:45 | 12:00 | 0:15 | | [22] Dohyun Kim, Koki Asahina, Yirong Kan, Renyuan Zhang and Yasuhiko Nakashima, "Power-Efficient Acceleration of GCNs on Coarse-Grained Linear Arrays" | | | | |
| 12:00 | 12:15 | 0:15 | | [26] Simon Friedrich, Robert Wittig, Emil Matus, Darius Grantz, Martin Zeller, Jens Benndorf and Gerhard Fettweis, "A 22 nm 10 TOPS Mixed-Precision Neural Network SoC for Image Processing with Energy-Efficient Dilated Convolution Support" | | | | |
| 12:15 | 12:25 | 0:10 | ASPIRE Session | | MINOWA Dai. "About the ASPIRE funding program and current open calls" | H. Amano | | |
| 12:25 | 13:45 | 1:20 | Lunch | | | | | |
| 13:45 | 14:45 | 1:00 | Poster Break | | | | | |
| 14:45 | 15:10 | 0:25 | Session XI : Parallel and Distributed Computing | | [15] Qi Li and Masato Edahiro, "Template-Based Automatic Library Function Generation with Halide for Compute-Intensive Simulink Models" | | | |
| 15:10 | 15:35 | 0:25 | | [29] Reoma Matsuo, Yuya Degawa, Hidetsugu Irie, Shuichi Sakai and Ryota Shioya, "Branch Divergence-Aware Flexible Approximating Technique on GPUs" | | | | |
| 15:35 | 15:50 | 0:15 | | [23] Daiki Saito, Siyi Hu and Yukinori Sato, "A Microservice Scheduler for Heterogeneous Resources on Edge-Cloud Computing Continuum" | | | | |
| 15:50 | 16:10 | 0:20 | Break | | | | | |
| 16:10 | 16:35 | 0:25 | Session XII : Accelerators | | [33] Sangjin Kim, Zhiyong Li, Soyeon Um, Wooyoung Jo, Sangwoo Ha, Sangyeob Kim and Hoi-Jun Yoo, "NoPIM: Functional Network-on-Chip Architecture for Scalable High-Density Processing-in-Memory-based Accelerator" | | | |
| 16:35 | 17:00 | 0:25 | | [31] Junha Ryu, Hankyul Kwon, Wonhoon Park, Zhiyong Li, Beomseok Kwon, Donghyeon Han, Dongseok Im, Sangyeob Kim, Hyungnam Joo, Minsung Kim and Hoi-Jun Yoo, "A Low-Power Neural Graphics System for Instant 3D Modeling and Real-Time Rendering on Mobile AR/VR Devices" | | | | |
| 17:00 | 17:15 | 0:15 | | [32] Muhammad Sulthan Mazaya, Eko Mursito Budi, Infall Syafalni, Nana Sutisna and Trio Adiono, "Reinforcement Learning Hardware Accelerator using Cache-Based for Optimized Q-Table Selection" | | | | |
| 17:15 | 17:40 | 0:25 | Session XIII : Poster Award and Closing Remarks | | | Y. Wada (Meisei Univ.) | R. Egawa (Tokyo Denki Univ.) | |