COOL Chips XVII Final Program

April 14, 2014 *Main Hall(7th Floor), Yokohama Joho Bunka Center*
(Yokohama Media & Communications Center)

13:00-14:30 **Special Session 1**
Co-chairs: Hiroyuki Tomiyama (Ritsumeikan University), Yuko Hara-Azumi (Tokyo Institute of Technology)

13:00-14:30 **Application-Specific Processors - Addressing High-Performance Computing Challenges**
Speaker: Masaaki Ideno (Synopsys)

Abstract: Embedded processors constantly increase their performance/power efficiency. At the same time, ever increasing algorithm complexity and low-power requirements make acceleration and processor offload ubiquitous in almost any SoC design. While hardwired logic is the traditional way accelerators have been implemented, multicore and application-specific processor (ASIP) solutions are gaining momentum because the advantages in programmability and time to market. Using the example of a pedestrian detection system as applied in modern automotive applications, we will illustrate how specialized ASIP architectures allow combining flexibility (e.g. faster time to market) and high-efficiency (performance/Watt). We will cover ASIP design methodology requirements, considering both architecture design, as well as the need for embedded software tools such as C-compiler, simulator, assembler, linker and debugger.

14:30-15:00 **Break**

15:00-16:30 **Special Session 2**
Co-chairs: Hiroyuki Tomiyama (Ritsumeikan University), Yuko Hara-Azumi (Tokyo Institute of Technology)

15:00-16:30 **Vivado HLS – High Level Synthesis for FPGA**
Speakers: Igor A. Kostarnov (Xilinx Japan)

Abstract: Compiling from C, C++ or SystemC into RTL is quickly becoming a common technique for complex algorithm implementation in silicon. This talk presents Vivado HLS – a high level synthesis tool from Xilinx that targets FPGA. Using FPGA changes how high level synthesis runs in a few ways. First, rather than generating a netlist of logic gates, HLS tool in FPGA should optimally use the existing coarser-grain resources. Then it should use the adopted way of joining the generated blocks in order to build a system on a chip and also such tool should well understand the trade-offs available in FPGA. In the presentation the basics of generating datapath, control and interfaces out of C code is described, paying special attention to the optimizations available for synthesis of high speed and efficient design. Optimal use of different levels of parallelism and eliminating memory bottlenecks is explained. Also the presentation covers the methodology for doing a software/hardware co-design in Vivado.

16:30-17:00 **Break**

17:00-18:30 **Special Session 3**
Co-chairs: Hiroyuki Tomiyama (Ritsumeikan University), Yuko Hara-Azumi (Tokyo Institute of Technology)

17:00-18:30 **A New Generation of Parallel Processing: Altera FPGAs as Accelerators for an OpenCL Platform**
Speakers: Dirk Seynhaeve (Altera, USA)

Abstract: A New Generation of Parallel Processing: Altera Instruction-set processors in search of more compute power have bumped into the barrier of power consumption. The solution for more performance is parallelism, however traditional programming languages were not very efficient to program parallel platforms. OpenCL is a standard C-based solution that elegantly solves the efficient programming of an entire heterogeneous platform. FPGAs are programmable devices, where application specific applications are implement as a custom circuit. This creates higher performance and lower power solutions compared to instruction set based processors. FPGAs are traditionally programmed with a class of tools labeled as hardware design tools, geared towards the physical implementation of the custom circuits. This tutorial will show the basics of OpenCL, an introduction to FPGAs, and how Altera has abstracted away a hardware design environment under a programmer-friendly OpenCL infrastructure. FPGAs as Accelerators for an OpenCL Platform

April 15, 2014 *Main Hall(7th Floor), Yokohama Joho Bunka Center*
(Yokohama Media & Communications Center)

9:30-9:50 **Session I**

9:30-9:50 **Welcome and Opening Remarks**
Chair: Hiroyuki Igura (NEC)

Hiroaki Kobayashi,	*Chair of the Organizing Committee*
Takatomo Enoki,	*President of the Electronics Society, IEICE*
Seiji Murozono	*Director of the Economic Affairs Bureau, City of Yokohama*

9:50-10:40 **Session II**

9:50-10:40 **Keynote Presentation 1**
Co-chairs: Masato Suzuki (Panasonic), Yukinori Sato (JAIST)

Programming the Internet of Things -- Combining Internet and Embedded Programming Models
Michael McCool (Intel, USA)

Abstract: The Internet of Things (IoT) can be defined most broadly as internet-enabled embedded computing. Things, able to sense and interact with the real world, must now also able to communicate over the internet with a potentially global reach. This broad definition of IoT covers a wide range of possible use cases, including but not limited to automotive computing, industrial, municipal, and environmental monitoring, home automation and security, smart appliances, wearables, and robotics. Communication may be machine-to-machine (M2M) or human-to-machine (H2M). Tiny devices need to be able to communicate and coordinate with data centers, and interact with users—often without displays of their own, and under severe power and form-factor constraints. IoT is also emerging in the context of existing web, tablet, and phone ecosystems. In this talk, I will discuss Intel's efforts to address the emerging IoT market with a range of suitable SoCs (both Atom and Quark based) scaling down to very low power for endpoints and gateways, novel dual operating system architectures combining real-time and Linux capabilities, and new programming models and tools for rapid development of applications. IoT "applications" may in fact span multiple devices, including sensor nodes, gateways, interface devices (such as smartphones, tablets, and laptops), and cloud services. Programming models developed for embedded devices need to be coordinated with programming models developed for web services and for developing rich user interfaces on smart phones. These programming models need to be accessible but at the same time need to deal with the realities of the limited resources available on IoT devices. This is a challenge, but the potential of IoT will be best unlocked by providing a wide range of developers the means to rapidly develop and bring their ideas to market.

10:40-11:50 **Break**

10:50-11:40 **Session III**

10:50-11:40 **Keynote Presentation 2**
Co-chairs: Hideharu Amano (Keio University), Akihiko Hashiguchi (Sony)

Future Trend and the chance of Reconfigurable Computing
Jay Kim (Samsung, Korea)

Abstract: Mobile devices become major computing resources in these days. The required computing has been dramatically changed corresponding to the increase of computing capability coming from technology improvement. It has been forced to increase the computing capacity while managing the battery life efficiently in the mobile market. The technical challenges to the mobile computing get more difficulties where the devices are wearable because of their requirements – better user experience, miniaturization, less skin temperature, and etc. In computing-wise, it is necessary to attack these requirements in two aspects. First, wearable computing still gives users enough computing power and ability to run the various applications. It is needed to handle different level of computing complexity and wide range of workload with different characteristics under limited battery capacity. In order to manage this situation efficiently, adaptive computing environment will be needed to catch up with this rapid change. At the same time, the superior position of the PPA (Power, Performance and Area) than other competitors will be essential for commercial success. Second, since wearable device is integrated into everyday objects that we wear constantly, its power consumption and heat dissipation become more important than those of hand-held devices. It is necessary to find the extremely energy efficient computing. In order to handle these two technical challenges and penetrate into the related market successfully, we need the proper solution to meet the similar PPA efficiency to HW while keeping scalability and flexibility. One of those candidates should be a reconfigurable computing.

11:40-11:50 **Break**

11:50-12:20 **Session IV: Poster Short Speeches**
Chair: Koji Hashimoto (Fukuoka University)

Poster 1 **An Adaptive Network-on-Chip Design to Support Directional Flow**
Kuei-Chung Changand, Bo-Yi Shiu (FengChia University, Taiwan)

Poster 2 **Instruction Steering Method by Utilizing Redundancy of Data Bit Width**
Ikumi Kaneko[1], Shoma Kawai[1], Ryotaro Kobayashi[1], Hajime Shimada[2] ([1]Toyohashi University of Technology, [2]Nagoya University)

Poster 3 **Early L0 Cache Access focusing on Useless Address Calculation**
Yuya Takeuchi[1], Hiroya Ochiai[1], Ryotaro Kobayashi[1], Hajime Shimada[2] ([1]Toyohashi University of Technology,[2] Nagoya University)

Poster 4 **On/Off Link Selection Schemes for Wireless 3D NoCs**
Go Matsumura[1], Michihiro Koibuchi[2], Hideharu Amano[1], Hiroki Matsutani[1] ([1]Keio University, [2]National Institute of Informatics)

Poster 5 **Voltage control considering the chip temperature in the three-dimensional stacked multi-core processors**
Yu Fujita, Yusuke Koizumi, Rie Uno, Hideharu Amano (Keio University)

Poster 6 **A Fine-grained Power Gating Control using Leakage Monitor by Linux Process Scheduler**
Atsushi Koshiba[1], Jun Tsukamoto[1], Motoki Wada[1], Ryuichi Sakamoto[1], Mikiko Sato[1], Tsubasa Kosaka[2], Kimiyoshi Usami[2], Hideharu Amano[3], Masaaki Kondo[4], Hiroshi Nakamura[4], Mitaro Namiki[1] ([1]Tokyo University of Agriculture and Technology, [2]Shibaura Institute of Technology, [3]Keio University, [4]The University of Tokyo)

Poster 7 **Power-efficient radix-8 FFT logic by elimination of intermediate sqrt-i multiplications**
Kohji Takano, Yasunao Katayama (IBM Research)

Poster 8 **A new low swing domino logic and an example design of a multiplier**
Sang-Yun Ahn, Minho Nam, Kyoungrok Cho (Chungbuk National University, Korea)

Poster 9 **A Configurable Finite Field Arithmetic Accelerator for Soft-cores**
Aiko Iwasaki, Keisuke Dohi, Yuichiro Shibata, Kiyoshi Oguri, Ryuichi Harasawa (Nagasaki University)

Poster 10 **Cool FPGA Implementation of Human Detection**
Masahito Oishi, Keisuke Dohi, Yuichiro Shibata, Kiyoshi Oguri (Nagasaki University)

Poster 11 **A Novel Idea of One Bit Resolution ADC for Small Analog Hardware Wireless Receivers**
Daisuke Kanemoto[1], Osamu Muta[2], Hiroshi Furukawa[2] Takahide Sato[1], Makoto Ohki[1] ([1]University of Yamanashi, [2]Kyushu University)

Poster 12 **A Pipelined Newton-Raphson Method for Floating Point Division and Square Root on Distributed Memory CGRAs**
Shuto Kurebayashi, Jun Yao, Yasuhiko Nakashima (Nara Institute of Science and Technology)

Poster 13 **Performance Tuning of a Global Shallow-water Atmospheric Model on Xeon Phi**
Masakazu Tanomoto[1], Jun Yao[1], Yasuhiko Nakashima[1], Yangtong Xu[2], Xinliang Wang[2], Wei Xue[2] ([1]Nara Institute of Science and Technology, [2]Tsinghua University, China)

Poster 14 **Tuning of a Breadth First based Triangle-counting by using Multi-threading**
Tatsuhiro Hirano, Jun Yao, Yasuhiko Nakashima (Nara Institute of Science and Technology)

Poster 15 **A Configurable Switch Mechanism for Random NoCs**
Seiichi Tade[1], Takahiro Kagami[1], Ryuta Kawano[1], Hiroki Matsutani[1], Michihiro Koibuchi[2], Hideharu Amano[1] ([1]Keio University, [2]National Institute of Informatics)

Poster 16 **Parallel Syndrome Generator for BCH Decoder**
Duk-Gyu Lim, Won-Jung Choi, Si-Byung Nam, Je-Hoon Lee (Kangwon National University, Korea)

Poster 17 **High-Speed SHA-1 Design with Carry-Save Adder**
Won-Ki Sung, Jae-Gyeong Jang, Won-Jung Choi, Je-Hoon Lee (Kangwon National University, Korea)

Poster 18 **Design of a tile based around an open-source processor with 65nm technology**
Mohamed Amine Boussadi, Thierry Tixier, Alexis Landrault, Jean-Pierre Derutin (Institut Pascal, France)

Poster 19 **Adding FPU to an open-source processor using user instructions**
Mohamed Amine Boussadi, Thierry Tixier, Alexis Landrault, Jean-Pierre Derutin (Institut Pascal, France)

Poster 20 **Design and Implementation of Flash Memory Aware MMU**
Hirotaka Kawata, Shuichi Oikawa (University of Tsukuba)

Poster 21 **Migration of Web Applications using Snapshot**

JinSeok Oh, Soo-Mook Moon (Seoul National University, Korea)

Poster 22 **Energy-Efficient Cache Coherence in Multi-processor with Efficient Broadcasts**
An Hsia, Chang-Jung Ku, Ching-Lin Hsu, Ching-Wen Chen (Feng Chia University. Taiwan)

Poster 23 **Implementation of Less Trap Architecture with Better Cache Utilization**
Motoharu Nakajima, Shuichi Oikawa (University of Tsukuba)

Poster 24 **Hybrid Main Memory Using Electrically- and Optically-Attached Memories**
Atsuya Okazaki, Nobuyuki Ohba, Yasunao Katayama (IBM Research)

Poster 25 **Hierarchical Parallel Processing of HEVC Encoder**
Hiroki Mikami, Keiji Kimura, Hironori Kasahara (Waseda University)

Poster 26 **iPIC: A Hardware Mechanism for Faster Interrupt Handling on Embedded Virtualizations**
Tomoaki Ukezono (Japan Advanced Institute of Science and Technology)

12:20-13:20 Lunch Time Break

13:20-13:40 Poster Open: 7th floor poster show room

13:40-14:30 Session V

13:40-14:30 **Keynote Presentation 3**
Co-chairs: Kohji Takano (IBM), Yusuke Nitta (Renesas Electronics)

SyNAPSE: Foundation of Future Neuronsynaptic Computing System
Jun Sawada (IBM, USA)

Abstract: SyNAPSE (Systems of Neuromorphic Adaptive Plastic Scalable Electronics) is a project aiming to build a brain-like computing system in the scale of mammalian brains. Our project team has been combining the principles of nano-science, neuroscience and super-computing to simulate and emulate the brain's abilities for sensation, perception, action, interaction and cognition, while rivaling its low power consumption and compact size. One key component of creating a scalable neurosynaptic computing is energy efficiency. In the phase one of this project, IBM demonstrated an ASIC neurosynaptic chip implemented with asynchronous circuits. This chip achieved an extremely low active-power consumption of 45pJ per spike. We also have created a neuron model that is simple enough to be implemented by a tiny circuit, but versatile enough to create various types of neurons. This neuron model can emulate logical and arithmetical functions, as well as biologically interesting neuron behaviors. Using this neuron model, we simulated a system of 5.3 x 10^11 neurons and 1.37 x 10^14 synapses on BlueGene/Q supercomputer. We envision that these technologies will be the foundation for a future scalable and flexible neurosynaptic computation system.

14:30-15:30 Break (Poster Open: 7th floor poster show room)

15:30-16:20 Session VI: Multi/Many Core
Co-chairs: Hiroyuki Takizawa (Tohoku University), Shintaro Izumi (Kobe University)

15:30-15:55 **Establishing a standard interface between multi-manycore and software tools - SHIM**

Masaki Gondo[1], Fumio Arakawa[2], Masato Edahiro[2] ([1]eSOL, [2]Nagoya University)

15:55-16:20 **Parallel Design of Control Systems Utilizing Dead Time for Embedded Multicore Processors**
Yuta Suzuki[1], Kota Sata[2], Junichi Kako[2], Kohei Yamaguchi[1], Fumio Arakawa[1], and Masato Edahiro[1] ([1]Nagoya University, [2]Toyota Motor)

16:20-16:30 Break

16:30-18:30 Session VII: Panel Discussions

Topics: Toward Wearable Computing Era, How COOL Chip Architectures and Tools will Evolve?
Organizer & Moderator: Fumio Arakawa (Nagoya University)
Panelists: Michael McCool (Intel, USA)
Soojung Ryu (Samsung, Korea)
Shumpei Kawasaki (Open Core Foundation, USA)
Hiroaki Tobita (Sony)

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9:30-10:20 **Session VIII**

9:30-10:20 **Keynote Presentation 4**
Co-chairs: Fumio Arakawa (Nagoya University), Yuki Kobayashi (Renesas Electronics)

Open Source Hardware Development Model and Old CPU
Shumpei Kawasaki (Open Core Foundation, USA)

Abstract: In 1965 Gordon E. Moore discovered a trend that the number of transistors on semiconductor integrated circuits doubles every 18 months. Semiconductor experts now predict this trend ends in 2013. From 2014 onward semiconductor industry needs innovations more than ever. While most disruptive innovation occurs from a new entrant concatenating prior inventions in her or his peculiar way, the chip hardware industry rarely shares design information with outsiders. To make things worse innovations within semiconductor companies are not likely either. Most corporations no longer assign resource to improve their own designs and license them from IP companies. The link of innovations is lost. To restore the lost link of innovations, people from all walks of life are exploring the possibility of open source hardware. A pinnacle of open source hardware today is open CPUs. These CPUs are coded in a Hardware Description Language (HDL) and uploaded to web for distribution with various licenses. Through logic synthesis, place and route and downloading they can be instantiated on FPGAs and later on ASICs. The presenter outlines perspectives on these grass-roots activities. In late 1980s the presenter worked on a settlement of intellectual property dispute between two companies one in US and one in Japan over instruction set architectures (ISAs). Through 1990s he held positions on CPU instruction and system architecture definitions. By juxtaposing corporate R&D experiences and observations of emerging open source hardware movement community, the presenter gives his perspectives on what should be in place for intellectual property management, design infrastructure, technological governance, licensing model, software compatibilities, and other things, if open source CPUs are to become a major element in future semiconductor. One important question is where should we seek open source CPU architecture…create new ISAs? or reuse existent ISAs?

10:20-10:40 **Break (Poster Open: 7th floor poster show room)**

10:40-11:20 **Session IX: Memories**
Co-chairs: Masanori Muroyama (Tohoku University), Akihiko Hashiguchi (Sony)

10:40-11:05 **Language Runtime Support for NVM/DRAM Hybrid Main Memory**
Gaku Nakagawa, Shuichi Oikawa (University of Tsukuba)

11:05-11:20 **A Low Power DRAM Refresh Control Scheme in Hybrid Memory Cube**
Ying Wang, Yinhe Han, Huawei Li (Chinese Academy of Sciences, China)

11:20-11:30 **Break (Poster Open: 7th floor poster show room)**

11:30-12:35 **Session X: Dependability**
Co-chairs: Akram Ben Ahmed (The University of Aizu), Hajime Shimada (Nagoya University)

11:30-11:55 **A Flexibly Fault-Tolerant FU Array Processor and its Self-Tuning Scheme to Locate Permanently Defective Unit**
Jun Yao, Yasuhiko Nakashima, Mitsutoshi Saito, Yohei Hazama, Ryosuke Yamanaka (Nara Institute of Science and Technology)

11:55-12:20 **A Globally Asynchronous Locally Synchronous DMR Architecture for Aggressive Low-Power Fault Toleration**
Yuttakon Yuttakonkit, Jun Yao, Yasuhiko Nakashima (Nara Institute of Science and Technology)

12:20-12:35 **Kernel Data Race Detection using Debug Register in Linux**
Yunyun Jiang, Yi Yang, Tian Xiao, Tianwei Sheng, Wenguang Chen (Tsinghua University, China)

12:35-13:40 Lunch Time Break

13:40-14:30 Session XI

13:40-14:30 **Keynote Presentation 5**
Co-chairs: Ryusuke Egawa (Tohoku University), Koyo Nitta (NTT Electronics)

Low Power High Performance Processors for Quantum Computing
Colin Williams (D-wave Systems, Canada)

Abstract: The media likes to portray quantum computing as being in a head to head race with high performance computing. In reality, we foresee ways for quantum computing to complement and enhance high performance computing and vice versa. In this talk I will describe D-Wave's approach to quantum computing including its operating principles, system architecture, evidence of quantumness, and report on our latest performance data, including the power efficiency of our processors. In particular, I will describe the latest version of D-Wave's quantum processor, and describe several examples of computational problems we have mapped to our architecture. I will then describe strategies for integrating our low power high performance quantum processors into mainstream high performance computing systems. As our quantum processors are naturally well suited to solving discrete combinatorial optimization, sampling, machine learning and artificial intelligence problems the talk should be of broad interest to computer scientists, physicists, and engineers with interests in a wide range of application areas.

14:30-14:40 Break (Poster Open: 7th floor poster show room)

14:40-15:30 Session XII: Low-Power Circuit Techniques
Co-chair: Makoto Ikeda (University of Tokyo), Akihiko Hashiguchi (Sony)

14:40-15:05 **A Perpetuum Mobile 32bit CPU with 13.4pJ/cycle, 0.14μA Sleep Current using Reverse Body Bias Assisted 65nm SOTB CMOS Technology**
Koichiro Ishibashi[1], Nobuyuki Sugii[2], Kimiyoshi Usami[3], Hideharu Amano[4], Kazutoshi Kobayashi[5], Cong-Kha Pham[1], Hideki Makiyama[2], Yoshiki Yamamoto[2], Hirofumi Shinohara[2], Toshiaki Iwamatsu[2], Yasuo Yamaguchi[2], Hidekazu Oda[2], Takumi Hasegawa[2], Shinobu Okanishi[2], Hiroshi Yanagita[2], Shiro Kamohara[2], Masaru Kadoshima[2], Keiichi Maekawa[2], Tomohiro Yamashita[2], Duc-Hung Le[1], Takumu Yomogita[1], Masaru Kudo[3], Kuniaki Kitamori[4], Shuya Kondo[5], Yuuki Manzawa[5] ([1]The University of Electro-Communications, [2]Low-power Electronics Association & Project, [3]Shibaura Institute of Technology, [4]Keio University, [5]Kyoto Institute of Technology)

15:05-15:30 **Embedded SRAM and Cortex-M0 Core with Backup Circuits Using a 60-nm**

Crystalline Oxide Semiconductor for Power Gating
Hikaru Tamura[1], Kiyoshi Kato[1], Takahiko Ishizu[1], Tatsuya Onuki[1], Wataru Uesugi[1], Takuro Ohmaru[1], Kazuaki Ohshima[1], Hidetomo Kobayashi[1], Seiichi Yoneda[1], Atsuo Isobe[1], Naoaki Tsutsui[1], Suguru Hondo[1], Yasutaka Suzuki[1], Yutaka Okazaki[1], Tomoaki Atsumi[1], Yutaka Shionoiri[1], Yukio Maehashi[1], Gensuke Goto[1], Masahiro Fujita[2], James Myers[3], Pekka Korpinen[4], Jun Koyama[1], Yoshitaka Yamamoto[1], Shunpei Yamazaki[1] ([1]Semiconductor Energy Laboratory, [2]The University of Tokyo, [3]ARM, [4]Nokia)

15:30-15:40 **Break**

15:40-16:55 **Session XIII: Power Optimization**
Co-chairs: Jun Yao (NAIST), Masaki Gondo (eSOL)

15:40-16:05 **Aggressive Use of Deep Sleep Mode in Low Power Embedded Systems**
Jun'ichi Segawa, Yusuke Shirota, Koichi Fujisaki, Tetsuro Kimura, Tatsunori Kanai (Toshiba)

16:05-16:30 **An Energy Optimization Method for Vector Processing Mechanisms**
Ye Gao, Masayuki Sato, Ryusuke Egawa, Hiroyuki Takizawa, Hiroaki Kobayashi (Tohoku University)

16:30-16:55 **A Fine Grained Power Management Supported by Just-In-Time Compiler**
Motoki Wada, Mikiko Sato, Mitaro Namiki (Tokyo University of Agriculture and Technology.)

16:55-17:05 **Break**

17:05-17:45 **Session XIV: NoC**
Co-chairs: Sugako Otani (Renesas Electronics), Yasutaka Wada (NEC)

17:05-17:30 **A Task-level Pipelined Many-SIMD Augmented Reality Processor with Congestion-aware Network-on-Chip Scheduler**
Gyeonghoon Kim, Seongwook Park, Kyuho Lee, Youchang Kim, Injoon Hong, Kyeongryeol Bong, Dongjoo Shin, Sungpill Choi, Junyoung Park, Hoi-Jun Yoo (KAIST, Korea)

17:30-17:45 **A Low Power NoC Router Using the Marching Memory Through Type**
Ryota Yasudo, Takahiro Kagami, Hideharu Amano, Yasunobu Nakase, Masashi Watanebe, Tsukasa Oishi, Toru Shimizu, Tadao Nakamura (Keio University)

17:45-18:05 **Poster Award and Closing Remark**
Makoto Ikeda, Program Committee Co-chair (University of Tokyo)