IEEE Symposium on Low-Power and High-Speed Chips

COOL Chips XVII

CALL FOR PARTICIPATION

COOL Chips is an International Symposium initiated in 1998 to present advancement of low-power and high-speed chips. The symposium covers leading-edge technologies in all areas of microprocessors and their applications.
The COOL Chips XVII is to be held in Yokohama on April 14-16, 2014, and is targeted at the architecture, design and implementation of chips with special emphasis on the areas listed below.

- **Low Power-High Performance Processors for Multimedia, Digital Consumer Electronics, Mobile, Graphics, Encryption, Robotics, Automotive, Networking, Medical, Healthcare, and Biometrics.**
- **Novel Architectures and Schemes for Single Core, Multi-Core, Embedded Systems, Reconfigurable Computing, Grid, Ubiquitous, Dependable Computing, GALS and Wireless.**
- **Cool Software including - Parallel Schedulers, Embedded Real-time Operating System, Binary Translations, Compiler Issues and Low Power Techniques.**

Dates and Location

April 14 (Mon) – 16 (Wed), 2014
Yokohama Joho Bunka Center, Yokohama, Japan
(Yokohama Media & Communications Center, Yokohama, Japan)

Keynote Presentations

- "Open Source Hardware Development Model and Old CPUs",
  Shumpei Kawasaki *(Open Core Foundation, USA)*
- "As Mobile Device Becomes Wearable,
  the Reconfigurable Processor Gets Cooler",
  Jay Kim *(Samsung, Korea)*
- "Programming the Internet of Things - Combining Internet and Embedded Programming Models",
  Michael McCool *(Intel, USA)*
- "SyNAPSE: Foundation of Future Neuronsynaptic Computing System", ***Jun Sawada*** *(IBM, USA)*
- "Low Power High Performance Processors for Quantum Computing", ***Colin Williams*** *(D-wave Systems, Canada)*

Panel Discussion

- Topics: "Toward Wearable Computing Era, How COOL Chip Architectures and Tools will Evolve? ",
  Organizer/Moderator:
  Fumio Arakawa *(Nagoya Univ., Japan)*

Special Sessions (invited lectures)

- "Application-Specific Processors – Addressing High-Performance Computing Challenges",
  Masaaki Ideno *(Synopsys, USA)*
- "Vivado HLS – High Level Synthesis for FPGA",
  Igor Kostarnov *(Xilinx Japan, Japan)*
- "A New Generation of Parallel Processing: Altera FPGAs as Accelerators for an OpenCL Platform",
  Dirk Seynhaeve *(Altera, USA)*

For more information, please visit <**http://www.coolchips.org/**>

Symposium Registration

In order to make a registration, please visit COOL Chips XVII web site: **< http://www.coolchips.org/ >**

- ***REGISTRATION FEES***

Registration Fees include a copy of the proceedings (copies of speakers' slides) of all plenary and technical sessions and special sessions presented on April 14-16, 2014.

	Early Registration by **March 31,** '14	Late Registration from April 1, '14
Member of any of IEEE, IEICE or IPSJ	40,000 yen	50,000 yen
Non-Member	50,000 yen	63,000 yen
Student (Member)	13,000 yen	17,000 yen
Student (Non-Member)	17,000 yen	20,000 yen

- ***PAYMENT***

- On-site cash payment
- Credit cards
  -- VISA/Master Cards are only acceptable

Detailed information is available on the web site.

Notes:
1. Credit card charges will be billed in Yen.
2. Personal checks, bank drafts, and traveler's checks are not acceptable.

Accommodations

- ***HOTEL RESERVATIONS***

A special group rate is available for COOL Chips XVII attendees for Hotel Monterey Yokohama and Hotel New Grand.

- ***CONTACT to***

COOL Chips XVII Organizing Committee Secretaries
E-mail:cool_XVII@coolchips.org http://www.coolchips.org/

Sponsored by the Technical Committees on Microprocessors and Microcomputers and Computer Architecture of the IEEE Computer Society.
In cooperation with the IEICE Electronics Society and IPSJ.

(As of March 13, 2014)