IEEE Symposium on Low-Power and High-Speed Chips

COOL Chips XIX

CALL FOR PARTICIPATION

COOL Chips is an International Symposium initiated in 1998 to present advancement of low-power and high-speed chips. The symposium covers leading-edge technologies in all areas of microprocessors and their applications.
The COOL Chips XIX is to be held in Yokohama on April 20-22, 2016, and is targeted at the architecture, design and implementation of chips with special emphasis on the areas listed below.

- **Low Power-High Performance Processors for Multimedia, Digital Consumer Electronics, Mobile, Graphics, Encryption, Robotics, Automotive, Networking, Medical, Healthcare, and Biometrics.**
- **Novel Architectures and Schemes for Single Core, Multi-Core, Embedded Systems, Reconfigurable Computing, Grid, Ubiquitous, Dependable Computing, GALS and Wireless.**
- **Cool Software including - Parallel Schedulers, Embedded Real-time Operating System, Binary Translations, Compiler Issues and Low Power Techniques.**

Dates and Location

April 20 (Wed) – 22 (Fri), 2016
Yokohama Joho Bunka Center, Yokohama, Japan
(Yokohama Media & Communications Center, Yokohama, Japan)

Keynote Presentations

- "Sub-pj per Operation Scalable Computing – the Next Challenge", ***Luca Benini*** *(ETHZ, Switzerland)*
- "Modality of CMOS Image Sensor Competition", ***Teruo Hirayama*** *(Sony, Japan)*
- "Power Optimization Leveraging FPGA and Voltage Regulator Chip Co-Design", ***Ashraf Lotfi*** *(Intel, USA)*
- "New Frontiers in Computing", ***Michael McCool*** *(Intel, USA)*
- "The Multiscale Dataflow Computing Chip", ***Oskar Mencer*** *(Imperial College London and Maxeler Technologies, UK)*
- "Cool Techniques for Hot Chips", ***Mateo Valero*** *(Barcelona Supercomputing Center, Spain)*

Invited Presentation

- "NanoBridge-based FPGA in Harsh Environments", ***Makoto Miyamura*** *(NEC, Japan)*

Panel Discussion

- Topics: "Computing and Communication Evolution for IoT Innovations"
  Organizer/Moderator: ***Hiroaki Nishi*** *(Keio University, Japan)*

Special Sessions (invited lectures)

- "Architectural Approaches to using STT-RAM for Low-Power Caches", ***Kiyoung Choi*** *(Seoul National University, Korea)*
- "Inter/Intra-Chip Optical Networks", ***Jiang Xu*** *(Hong Kong University of Science and Technology, China)*

For detailed and up-to-date information, please visit
< http://www.coolchips.org/ >

Symposium Registration

In order to make a registration, please visit COOL Chips XIX web site: **< http://www.coolchips.org/ >**

- ***REGISTRATION FEES***

Registration Fees include a copy of the proceedings (copies of speakers' slides) of all plenary and technical sessions and special sessions presented on April 20-22, 2016.

(including tax)	Early Registration by **April 7,** '16	Late Registration from April 8, '16
Member of any of IEEE, IEICE or IPSJ	40,000 yen	50,000 yen
Student (Member)	13,000 yen	17,000 yen
Life/Retired (Member)	13,000 yen	17,000 yen
Non-Member	50,000 yen	63,000 yen
Student (Non-Member)	17,000 yen	20,000 yen

- ***PAYMENT***

- On-site cash payment
- Credit cards
  -- VISA/Master Cards are only acceptable

Detailed information is available on the web site.

Notes:
1. Credit card charges will be billed in Yen.
2. Personal checks, bank drafts, and traveler's checks are not acceptable.

Accommodations

- ***HOTEL RESERVATIONS***

A special group rate is available for COOL Chips XIX attendees for Hotel Monterey Yokohama and Hotel New Grand.

- ***CONTACT to***

COOL Chips XIX Organizing Committee Secretaries
E-mail:cool_XIX@coolchips.org http://www.coolchips.org/

Sponsored by the Technical Committees on Microprocessors and Microcomputers and Computer Architecture of the IEEE Computer Society. (approval pending)
In cooperation with the IEICE Electronics Society and IPSJ.

(As of March 23, 2016)