Final Program

April 19, 2017 *Main Hall(7th Floor), Yokohama Joho Bunka Center*
(Yokohama Media & Communications Center)

13:30-15:00 **Special Invited Lecture 1**
Chair: Tohru Ishihara (Kyoto Univ.)

13:30-15:00 **TrueNorth: A Neurosynaptic Integrated Circuit with 1 Million Spiking Digital Neurons**
Yutaka Nakamura (IBM Research)

Abstract: Inspired by the brain's structure, we have developed an efficient, scalable, and flexible non–von Neumann architecture that leverages contemporary silicon technology. To demonstrate, we built TrueNorth, a 5.4-billion-transistor chip with 4096 neurosynaptic cores interconnected via an intra-chip network that integrates 1 million programmable spiking neurons and 256 million configurable synapses. Chips can be tiled in two dimensions via an inter-chip communication interface, seamlessly scaling the architecture to a cortex-like sheet of arbitrary size. The architecture is well suited to many applications that use complex neural networks in real time, for example, multi object detection and classification. With 400-pixel-by-240-pixel video input at 30 frames per second, the chip consumes 63 mW.

15:00-15:30 **Break**

15:30-17:00 **Special Invited Lecture 2**
Chair: Tohru Ishihara (Kyoto Univ.)

15:30-17:00 **Design and Test of Low-Voltage Micro-Electrode-Dot-Array Digital Microfluidic Biochips**
Tsung-Yi Ho (National Tsing Hua University, Taiwan)

Abstract: A digital microfluidic biochip (DMFB) is an attractive technology platform for automating laboratory procedures in biochemistry. However, today's DMFBs suffer from several limitations: (i) constraints on droplet size and the inability to vary droplet volume in a fine-grained manner; (ii) the lack of integrated sensors for real-time detection; (iii) the need for special fabrication processes and reliability/yield concerns. To overcome the above problems, DMFBs based on a micro-electrode-dot-array (MEDA) architecture, and fabricated using a TSMC 350 nm process, have recently been demonstrated. This presentation will first describe a biochemistry synthesis approach for such MEDA biochips. This synthesis method targets operation scheduling, module placement, routing of droplets of various sizes, and diagonal movement of droplets in a two-dimensional array. Simulation results using benchmarks and experimental results using a fabricated MEDA biochip will be presented to demonstrate the effectiveness of the proposed co-optimization technique. Finally, the presentation will describe an efficient built-in self-test (BIST) solution for MEDA biochips. Simulation results based on HSPICE and experiments using fabricated MEDA biochips will highlight the effectiveness of the proposed BIST architecture.

April 20, 2017 *Main Hall(7th Floor), Yokohama Joho Bunka Center*
(Yokohama Media & Communications Center)

9:30-9:50 **Session I**

9:30-9:50 **Welcome and Opening Remarks**
Chair: Yuki Kobayashi (NEC)

Hiroaki Kobayashi,	*Chair of the Organizing Committee*
Allen J. Baum	*Chair of IEEE/CS TCMM*
Hironori Kasahara	*IEEE/CS 2017 President-Elect*
Hiromi Oohashi	*President of IEICE/ES*

9:50-10:40 **Session II**

9:50-10:40 **Keynote Presentation 1**
Co-chairs: Hiroaki Kobayashi (Tohoku Univ.), Masato Suzuki (Socionext)

The Sunway TaihuLight Supercomputer and the Shenwei 26010 Processor: the Design and the Performance
Haohuan Fu (National Supercomputing Center in Wuxi, China)

The Sunway TaihuLight supercomputer is the world's first system with a peak performance greater than 100 PFlops, and a parallel scale of over 10 million cores. In contrast with other existing heterogeneous supercomputers, which include both CPU processors and PCIe-connected many-core accelerators (NVIDIA GPU or Intel MIC), the computing power of TaihuLight is provided by a homegrown many-core SW26010 CPU that includes both the management processing elements (MPEs) and computing processing elements (CPEs) in one chip. With 260 processing elements in one CPU, a single SW26010 provides a peak performance of over three TFlops. To alleviate the memory bandwidth bottleneck in most applications, each CPE comes with a scratch pad memory, which serves as a user-controlled cache. To support the parallelization of programs on the new many-core architecture, in addition to the basic C/C++ and Fortran compilers, the system provides a customized Sunway OpenACC tool that supports the OpenACC 2.0 syntax and supports the management of parallel tasks. This talk introduces and discusses the design philosophy behind both the many-core processor and the 10-million-core system. The application performance on both the processor and the system would also be discussed.

10:40-11:05 **Session III: High Performance Processor**
Chair: Kotaro Shimamura (Hitachi)

10:40-11:05 **SPARC64™ XII: Fujitsu's latest 12 Core Processor for Mission Critical Servers**
Takumi Maruyama (Fujitsu)

11:05-11:25 **Break**

11:25-11:55 **Session IV: Poster Short Speeches**
Chair: Koji Hashimoto (Fukuoka Univ.)

Poster 1 **A Flip-Flop with High Soft-error Tolerance and Small Power and Delay Overheads**
Kodai Yamada, Haruki Maruoka, Jun Furuta, Kazutoshi Kobayashi (Kyoto Institute

of Technology)

Poster 2 **Adaptive Energy-Aware Cache Coherence Protocol for Virtual Machines**
Chia-Hsiang Chung, Jian-Cheng Huang, Ching-Wen Chen (Feng Chia Univ., Taiwan)

Poster 3 **A Dynamic Frequency Scaling Approach for Reducing Product of Energy and Delay**
Jian-Cheng Huang, Chia-Hsiang Chung, Ching-Wen Chen (Feng Chia Univ., Taiwan)

Poster 4 **Zynq-based ARM-FPGA Cooperative Platform for Maximum Stack Usage Analysis in Embedded Systems**
Kiho Choi, Seong Seop Kim, Jeonghun Cho, Daejin Park (Kyungpook National Univ., Korea)

Poster 5 **Basic Design of OS Scheduler for SOTB CPU "GC-SOTB" to Reduce Power Consumption**
Shinsuke Hamada, Athushi Koshiba, Mitaro Namiki (Tokyo Univ. of Agriculture and Technology)

Poster 6 **Power Optimization for CGRA with Control of Variable Pipeline and Body Bias Voltage**
Takuya Kojima, Naoki Ando, Hayate Okuhara, Ng. Anh Vu Doan, Hideharu Amano (Keio Univ.)

Poster 7 **A Scalable Ising Model Implementation on an FPGA**
Kasho Yamamoto, Shinya Takamaeda-Yamazaki, Masayuki Ikebe, Tetsuya Asai, Masato Motomura (Hokkaido Univ.)

Poster 8 **CNN Acceleration on Multi-FPGA System**
Kazusa Musha, Hideharu Amano (Keio Univ.)

Poster 9 **Implementation of the PIC method's aggregation process on a SoC FPGA to avoid RAW hazards using reduction**
Hiroyuki Noda[1], Ryotaro Sakai[1], Takaaki Miyajima[2], Naoyuki Fujita[2], Hideharu Amano[1] ([1]Keio Univ., [2]Japan Aerospace Exploration Agency)

Poster 10 **Performance Evaluation of the Generalized De Bruijn Graph with Deflection Routing**
Tomohiro Totoki[1], Hiroshi Nakahara[1], Michihiro Koibuchi[2], Hideharu Amano[1] ([1]Keio Univ., [2]National Institute of Informatics)

11:55-13:15 Lunch Time Break

13:15-13:35 Poster Open: 7th floor poster show room

13:35-14:25 Session V

13:35-14:25 **Keynote Presentation 2**
Co-chairs: Akihiko Hashiguchi (Sony), Kunio Uchiyama (Hitachi)

New Era of Electrification and Vehicle Intelligence
Haruyoshi Kumura (Nissan Motor)

Abstract: As the global demand for personal mobility grows continuously, the automotive industry needs to accelerate the development of solutions for the social

problems such as environment, energy, resources, traffic accidents and urban congestions. The vehicle electrification and intelligence are key technologies to resolve these social problems. Autonomous drive system technology installed in the latest vehicle will be shared. The examples of recent development for future autonomous drive system will be also shared. Technical issues and challenges for semiconductor will be discussed.

14:25-15:25 **Break (Poster Open: 7th floor poster show room)**

15:25-16:15 **Session VI: Artificial Intelligence**
Co-chairs: Shinya Takamaeda-Yamazaki (Hokkaido Univ.), Kazushi Kawamura (Waseda Univ.)

15:25-15:50 **An Energy-Efficient Deep Learning Processor with Heterogeneous Multi-Core Architecture for Convolutional Neural Networks and Recurrent Neural Networks**
Dongjoo Shin, Jinmook Lee, Jinsu Lee, Juhyoung Lee, Hoi-Jun Yoo (KAIST, Korea)

15:50-16:15 **Intelligence Boosting Engine (IBE): a Hardware Accelerator for Processing Sensor Fusion and Machine Learning Algorithm for a Sensor Hub SoC**
Minkwan Kee[1], Seung-Jin Lee[1], Hyun-Su Seon[2], Jongsung Lee[2], Gi-Ho Park[1] ([1]Sejong University, [2]Standing-egg, Korea)

16:15-16:30 **Break**

16:30-18:00 **Session VII: Panel Discussions**

Topics: "Cool chips for the next decade"
Organizer & Moderator: Hideharu Amamo (Keio Univ.)
Panelists: Tadao Nakamura (Keio Univ.)
Hiroaki Kobayashi (Tohoku Univ.)
Hironori Kasahara (Waseda Univ.)
Yoshiaki Hagiwara (AIPS)
Jeffrey L. Burns (IBM Research)
David Brash (ARM)

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9:30-10:20 **Session VIII**

9:30-10:20 **Keynote Presentation 3**
Co-chairs: Ryusuke Egawa (Tohoku Univ.), Yuki Kobayashi (NEC)

ARM: Scaling New Heights
David Brash, Nigel Stephens (ARM)

Abstract: In 2011 ARM announced ARMv8-A which included the new 64-bit AArch64 execution state, a step change for the architecture. ARMv8-A is now well established across a wide range of devices spanning consumer and enterprise markets. Fujitsu's 2016 announcement that Japan's Post-K supercomputer would be based on ARMv8-A, followed by the disclosure of ARM's next-generation Scalable Vector Extension (SVE) at HotChips, illustrates how the ARM processor architecture now scales from the smallest IoT devices to the largest HPC systems. This talk will focus on the evolution of the high-end ARMv8-A architecture, its recent enhancements for enterprise solutions, and its building momentum in high-performance scientific computing — all as part of an expanding collaboration between hardware, software and architecture partners. Key aspects of SVE will be outlined as well as the work to promote a thriving development ecosystem for tools, middleware and applications.

10:20-10:40 **Break (Poster Open: 7th floor poster show room)**

10:40-11:30 **Session IX**

10:40-11:30 **Keynote Presentation 4**
Co-chairs: Takuya Nakaike (IBM), Yukinori Sato (Tokyo Institute of Technology)

POWER9 Design Innovations
Jeffrey L. Burns (IBM Research, USA)

Abstract: Cognitive computing has become a major trend, driving the rapid development of new applications and workloads. The upcoming IBM POWER9 implements several new features targeting these emerging cognitive workloads. Adding new and improved cognitive capabilities requires higher levels of performance and energy-efficiency in the IT infrastructure. The maturation of semiconductor scaling has made delivering these higher levels more challenging; reliance on scaling alone is insufficient. Because of these trends, innovation in design and architecture is crucial. Innovations are required to improve power-performance of processors, e.g., by increasing the ability to dynamically adjust operating points without compromising the reliability of the computations. Accelerators will increasingly be needed to improve the power/performance of systems. To enable practical accelerator integration, system architectures must be designed up-front to incorporate heterogeneous components such as today's GPUs, as well as future accelerators for cognitive applications. In this presentation I will describe these trends, the POWER9 innovations that address them, and areas of research towards future systems.

11:30-11:55 **Session X: Circuits on SOI**
Chair: Yuetsu Kodama (Riken)

11:30-11:55 **Leveraging Asymmetric Body Bias Control for Low Power LSI Design**
Hayate Okuhara, Akram Ben Ahmed, Johannes Maximilian Kuehn, Hideharu Amano (Keio Univ.)

11:55-13:35 Lunch Time Break

13:35-14:15 Session XI: Memory Architectures
Co-chairs: Sugako Otani (Renesas), Hajime Shimada (Nagoya Univ.)

13:35-14:00 **An Adjacent-Line-Merging Writeback Scheme for STT-RAM Last-Level Caches**
Masayuki Sato, Zentaro Sakai, Ryusuke Egawa, Hiroaki Kobayashi (Tohoku Univ.)

14:00-14:15 **An Application-adaptive Data Allocation Method for Multi-channel Memory**
Takuya Toyoshima, Masayuki Sato, Ryusuke Egawa, Hiroaki Kobayashi (Tohoku Univ.)

14:15-14:35 Break (Poster Open: 7th floor poster show room)

14:35-15:25 Session XII: Image Processing
Co-chairs: Hidetoshi Matsumura (Fujitsu Labs.), Hiroyuki Takizawa (Tohoku Univ.)

14:35-15:00 **A 120 fps High Frame Rate Real-time HEVC Video Encoder with Parallel Configuration Scalable to 4K**
Yuya Omori, Takayuki Onishi, Hiroe Iwasaki, Atsushi Shimizu (NTT)

15:00-15:25 **A 216 GOPS Flexible WDR Image Processor for ADAS SoC**
Mihir Mody, Hetul Sanghvi, Niraj Nandan, Shashank Dabral, Rajasekhar Allu, Rajat Sagar, Kedar Chitnis, Jason Jones, Brijesh Jadhav, Sujith Shivalingappa, Aish Dubey (Texas Instruments, USA)

15:25-15:45 Break (Poster Open: 7th floor poster show room)

15:45-16:50 Session XIII: Low Power SoC and Software
Co-chairs: Yasutaka Wada (Meisei Univ.), Masanori Muroyama (Tohoku Univ.)

15:45-16:10 **Low-Power Multi-Sensor System with Task Scheduling and Autonomous Standby Mode Transition Control for IoT Applications**
Masanori Hayashikoshi[1], Hideyuki Noda[1], Hiroyuki Kawai[2], Koji Nii[1], Hiroyuki Kondo[1] ([1]Renesas Electronics, [2]Tokushima Bunri Univ.)

16:10-16:25 **Body Bias Control for Renewable Energy Source with a High Inner Resistance**
Keita Azegami, Hayate Okuhara, Hideharu Amano (Keio Univ.)

16:25-16:50 ***Blackghost*: An Ultra-Low-Power All-In-One 28nm CMOS SoC for Internet-of-Things**
Y. Pu, G. Samson, C. Shi, D. Park, K. Easton, R. Beraha, J. Hadi, M. Lin, E. Arvelo, J. Fatehi, J. Kumar, M. Derkalousdian, P. Aghera, A. Newham, H. Sheraji, K. Chatha, R. McLaren, V. Ganesan, S. Namasivayam, D. Butterfield, R. Shenoy, R. Attar (Qualcomm Research, USA)

16:50-17:00 Break

17:00-17:20 Poster Award and Closing Remark
Makoto Ikeda, Program Committee Co-chair (Univ. of Tokyo)