IEEE Symposium on Low-Power and High-Speed Chips

COOL Chips XIII

CALL FOR PARTICIPATION

COOL Chips is an International Symposium initiated in 1998 to present advancement of low-power and high-speed chips. The symposium covers leading-edge technologies in all areas of microprocessors and their applications.
The COOL Chips XIII is to be held in Yokohama on April 14-16, 2010, and is targeted at the architecture, design and implementation of chips with special emphasis on the areas listed below.

- **Low Power-High Performance Processors, "Eco-Processors", for Multimedia, Digital Consumer Electronics, Mobile, Graphics, Encryption, Robotics, Automotive, Networking, Medical, Healthcare, and Biometrics.**
- **Novel Architectures and Schemes for Single Core, Multi-Core, Embedded Systems, Reconfigurable Computing, Grid, Ubiquitous, Dependable Computing, GALS and Wireless.**
- **Cool Software including - Parallel Schedulers, Embedded Real-time Operating System, Binary Translations, Compiler Issues and Low Power Techniques.**

Dates and Location

April 14-16, 2010

Yokohama Joho Bunka Center, Yokohama, Japan

(Yokohama Media & Communications Center, Yokohama, Japan)

Keynote Presentations

- "Device Cloud Computing",
  Shih-Wei Liao *(Google Inc., USA)*
- "Electrodes on Chips for Life Science Applications, Solutions for Fully-integrated Systems",
  Carlotta Guiducci *(EPFL, Switzerland)*
- "POWER7: IBM's Next Generation Server Processor",
  Jim Kahle *(IBM Corp., USA)*
- "Super Camera Technology at NHK",
  Hiroshi Shimamoto *(NHK Eng. Services, Inc., Japan)*
- "High Performance and Low Power Processor for PETA Scale Computing", ***Iwao Yamazaki*** *(Fujitsu, Japan)*
- "NVIDIA Tegra, Achitecture of Low Power",
  Gordon Grigor *(NVIDIA, USA)*

Invited Presentation

- "Multi-Voltage Based Low Power Design Trends and Verification Techniques",
  Progyna Khondkar *(Nihon Synopsys, Japan)*

Panel Discussion

- Topics: "What is the Future Multi-layer Co-design of Computer Systems?",
  organizer: ***Fumio Arakawa*** *(Renesas Tech., Japan)*

Special Sessions (invited lectures)

- "Convergence of Design and Fabrication Technologies, a Key Enabler for Multi-layer HW-SW Integration",
  Ahmed Jerraya *(CEA-LETI, France)*
- "Achieving Fast Design Closure Using Networks on Chips", ***Srinivasan Murali*** *(EPFL/iNoCs, Switzerland)*
- "Resolving the Grand Paradox: Low Energy and Full Programmability in 4G Mobile Baseband SOCs",
  Chris Rowen *(Tensilica, USA)*

For more information, please visit <**http://www.coolchips.org/**>

Sponsored by the Technical Committees on Microprocessors and Microcomputers and Computer Architecture of the IEEE Computer Society. In cooperation with the IEICE Electronics Society, ACM SIGARCH and IPSJ.

Symposium Registration

In order to make a registration, please use COOL Chips XIII REGISTRATION FORM on web site at

< http://www.coolchips.org/ >

REGISTRATION FEES

Registration Fees include a copy of the proceedings (copies of speakers' slides) of all plenary and technical sessions and special sessions presented on April 14-16, 2010.

	Early Registration by **March 31**, '10	Late Registration from April 1, '10
Member of any of IEEE IEICE, IPSJ or ACM	30,000 yen	36,000 yen
Non-Member	38,000 yen	46,000 yen
Student (Member)	10,000 yen	12,000 yen
Student (Non-Member)	13,000 yen	16,000 yen

PAYMENT AND REMITTANCE

For attendees from inside Japan:
- Fees should be prepaid with a bank transfer by April 9.

For attendees from outside Japan:
- VISA or MasterCard are acceptable.

Detailed information is available on the web site.

Notes:
1. Credit card charges will be billed in Yen.
2. Personal checks, bank drafts, and traveler's checks are not acceptable.

Accommodations

HOTEL RESERVATIONS

A special group rate is available for COOL Chips XIII attendees for Hotel Monterey Yokohama and Hotel New Grand.

CONTACT to

COOL Chips XIII Organizing Committee Secretaries
E-mail:cool_XIII@coolchips.org http://www.coolchips.org/

(As of March 17, 2010)