Final Program

April 14, 2010 *Main Hall(7th Floor), Yokohama Joho Bunka Center*
(Yokohama Media & Communications Center)

10:00-12:00 **Special Session 1**
Co-chairs: Hiroyuki Tomiyama (Nagoya Univ.), Yuko Azumi (Nagoya University / Ritsumeikan Univ.)

10:00-12:00 **Resolving the Grand Paradox: Low Energy and Full Programmability in 4G Mobile Baseband SOCs**
Speaker: Chris Rowen (Tensilica, USA)

Abstract: Continued improvement in silicon density, combined with acceleration in mobile baseband terminals bandwidth and volume is driving basic change for highly integrated systems. But mobile baseband SOCs face an essential paradox - on one hand, increased mobility dictates smaller batteries, longer battery life and improved energy efficiency. On the other hand, the complexity of new baseband standards like LTE - plus the multimedia, network protocols and application services enabled by fast baseband - dictate increased programmability, ubiquitous multi-core and more software layers. How could this possibly work? This talk describes practical successes for ultra-low energy processors used for LTE PHY subsystem designs achieving 150Mbps data rates in less than 250mW. And resolving this paradox has a domino effect on wireless infrastructure, DTV and wired communications.

12:00-13:20 **Lunch Time Break**

13:20-15:20 **Special Session 2**
Co-chairs: Hiroyuki Tomiyama (Nagoya Univ.), Yuko Azumi (Nagoya University / Ritsumeikan Univ.)

13:20-15:20 **Convergence of Design and Fabrication Technologies, a Key Enabler for Multi-layer HW-SW Integration**
Speaker: Ahmed Jerraya (CEA-LETI, France)

Abstract: The last decade was dominated by HW-SW convergence where designers learned to combine hardware and software design to cope with the increased demand of lower cost and increased performances. This starting decade will be dominated by the convergence between design technology (HW and SW) and fabrication technologies. In fact more and more designs require a deep knowledge of technology characteristics to reach the required performances. On the other side, design technologies are more and more used to overcome fabrication process imperfection and to improve yield.
This talk will first explain the achievements in HW-SW convergence and SoC design. Then, it will address the fabrication technology trends and challenges to deal with this convergence.

15:20-15:50 **Break**

15:50-17:50 **Special Session 3**
Co-chairs: Hiroyuki Tomiyama (Nagoya Univ.), Yuko Azumi (Nagoya University /

Ritsumeikan Univ.)

15:50-17:50 **Achieving Fast Design Closure Using Networks on Chips**
Speaker: Srinivasan Murali (EPFL/iNoCs, Switzerland)

Abstract: The growing complexity of Systems on Chips (SoCs) and Chip Multi-Processors (CMPs) is requiring communication resources that can only be provided by a highly-scalable Networks on Chip (NoC) based communication infrastructure. Developing NoC-based systems tailored to a particular application domain is important for achieving high-performance, energy-efficient customized solutions. To achieve early time-to-market, it is important to have a CAD tool flow that automates most of the time-intensive design steps. In this talk, I will first present the basics of NoCs: covering several aspects including topology design, routing and flow control. Then, I will show why a CAD flow is crucial in solving the NoC design problem efficiently and for achieving design closure.

April 15, 2010 *Main Hall(7th Floor), Yokohama Joho Bunka Center*
(Yokohama Media & Communications Center)

9:30-11:30 **Session I**

9:30-9:50 **Welcome and Opening Remarks**
Chair: Kazumasa Suzuki (Renesas Electronics)

Tadao Nakamura,	*Chair of the Organizing Committee*
Donald. A. Draper,	*TCMCOMP Chair*
Kazuya Masu,	*President of Electronics Society, IEICE*
Fumiko Hayashi,	*Mayor of Yokohama City*

9:50-10:40 **Keynote Presentation 1**
Co-chairs: Michinori Nishihara (AIPS), Kouji Hosokawa (IBM)

POWER7: IBM's Next Generation Server Processor
Jim Kahle (IBM, USA)

Abstract: Jim Kahle will present a technical Overview of new Power7 system that IBM launched early this year. Jim will start with a brief recap of IBM innovation and Power History. Jim will then cover technical aspects of the chip, from a new core to enhanced SMP interconnect that includes eDRAM. As chief engineer of the Power7 chip, Jim has unique insight and experience of how create a world class design. It will become evident how Jim's experience in creating chips from laptops, workstations, game consoles to servers can create a break through design. Power7 flexibility from world class single thread execution to 4 way SMT shows how Power7 will power the workload of today and tomorrow. Jim will also describe the first systems that have been announced around this exciting chip. Power7 shows how IBM is a technical leader in server class designs and how it exploits leading edge technology to be a leader in the Industry.

10:40-11:30 **Keynote Presentation 2**
Co-chairs: Yoshio Hirose (Fujitsu Laboratories), Yasuo Unekawa (Toshiba)

High Performance and Low Power Processor for PETA Scale Computing
Iwao Yamazaki (Fujitsu, Japan)

Abstract: SPARC64VIIIfx is a new processor developed for use in peta-scale computing systems. The chip is fabricated in Fujitsu's 45nm CMOS technology, has 8 cores that run at a speed of 2GHz, and achieves a peak performance of 128GFLOPS. The entire chip consumes only 58W of power when executing a maximum power program.
The design goals for this processor were high performance, low power consumption, and high reliability. High performance is achieved via architectural enhancements. Low power consumption is realized through the selection of a moderate chip frequency, which allows dynamic current to be significantly reduced via extensive clock gating and data bus gating. Power consumption is also reduced by the use of a water cooling system; water cooling enables a lower CPU operating temperature, which reduces leakage current. The lower operating temperature also enables high reliability by minimizing the risk of chip failures. RAS features adapted from mission critical servers further increase reliability by protecting against both chip failures and soft errors.
This presentation introduces the high-performance architecture of SPARC64VIIIfx and low-power techniques, with a focus on techniques for reducing the power

consumption of the L1 and L2 caches

11:30-11:50 **Break**

11:50-12:20 **Session II : Poster Short Speeches**
Chair: Masanori Muroyama (Tohoku University)

Poster 1 **A High Performance Range-Matching Circuit Design for Packet Filter**
Hsiang-Yu Lu, Yen-Jen Chang (National Chung Hsing Univ., Taiwan)

Poster 2 **Flexible Hardware Architecture of Hierarchical K-Means Clustering for Large Cluster Number**
Tse-Wei Chen, Shao-Yi Chien (National Taiwan Univ., Taiwan)

Poster 3 **Design of Caches with Conflict Misses Reduction in Power-aware Embedded Systems**
Ching-Wen Chen, Chang-Jung Ku, Chien-Fu Chen (Feng Chia Univ., Taiwan)

Poster 4 **A Two-Step Partial-Byte-Based Computation Scheme for a Low-Power High-Performance Block Matching Circuit**
Tsung-Yi Wu[1], How-Rern Lin[2], Shi-Yi Huang[1], You-Da Lin[1], Jing-Wen Shi[1] ([1]National Changhua Univ. of Education, [2]Providence Univ., Taiwan)

Poster 5 **System-Level Power Estimation Platform for Network-on-Chip**
Kuei-Chung Chang, Chiu-Han Liao (Feng-Chia Univ., Taiwan)

Poster 6 **Reducing Leakage Power by Controlling Cooling Fan Speed**
A Ra Cho, Hyung Beom Jang, Jun Hee Lee, Sung Woo Chung (Korea Univ., Korea)

Poster 7 **Configuration power reduction effect of an ORGA with analog configuration**
Yuji Aoyama, Minoru Watanabe (Shizuoka Univ.)

Poster 8 **A 16-bit RISC Processor with 4.18pJ/cycle at 0.5V Operation**
Dan Kuroda, Hiroshi Fuketa, Masanori Hashimoto, Takao Onoye (Osaka Univ.)

Poster 9 **Priority-based Network-on-Chip for Multi-Core SoCs**
Kuei-Chung Chang and Ing-Ming Liao (Feng-Chia Univ., Taiwan)

Poster 10 **Power reduction method using negative logic implementation**
Retsu Moriwaki, Minoru Watanabe (Shizuoka Univ.)

Poster 11 **4×4-Bit Array Multiplier using Two Phase Clocked Adiabatic Static CMOS Logic**
Nazrul Anuar, Yasuhiro Takahashi, Toshikazu Sekine (Gifu Univ.)

Poster 12 **Area Optimization of FU Array in Low-Power Accelerators**
Takuya Iwakami, Munehisa Agari, Kazuhiro Yoshimura, Takashi Nakada, Yasuhiko Nakashima (Nara Inst. of Science and Technology)

Poster 13 **Implementation and Evaluation of a Superscalar Processor Based on Dynamic Adaptive Redundant Architecture**
Ryoji Watanabe[1], Jun Yao[1], Hajime Shimada[1], Kazutoshi Kobayashi[2] ([1]Nara Inst. of Science and Technology, [2]Kyoto Inst. of Technology)

Poster 14 **Multi-Frame Processing Architecture for Coarse-grained Reconfigurable Image Stream Processor**
Teng-Yuan Cheng, Tse-Wei Chen, Shao-Yi Chien (National Taiwan Univ., Taiwan)

Poster 15 **Design of a Data Cache Supporting Write Back Mode for Asynchronous Embedded Processor**
Jong-Min Park[1], Seok-man Kim[1], Myoung-Hoon Oh[2], Kyoungrok Cho[1] ([1]Chungbuk National Univ., [2]ETRI, Korea)

Poster 16 **Mitigation of Cache Writeback Overhead Focusing on Data Locality**
Hayato Usui, Yoshio Shimomura, Ryotaro Kobayashi (Toyohashi Univ. of Technology)

Poster 17 **Explicit-Pulsed Pass-Gate Level-Converting Flip-Flop For Low-Power Applications**
Wang-Ling Goh, Kiat-Seng Yeo, Myint-Wai Phyu (Nanyang Technological Univ.)

12:20-13:40 Lunch Time Break

13:40-14:30 Session III:
Co-chairs: Fumio Arakawa (Renesas Electronics), Akihiko Hashiguchi (Sony)

13:40-14:30 **Keynote Presentation 3**
Super Camera Technology at NHK
Hiroshi Shimamoto (NHK Engineering Services)

Abstract: Television has realized human demand to see far scenes in real. The progress of camera technology is now overcoming limitation of human vision, such in spatial resolution, temporal resolution, and sensitivity. In this talk, we will introduce three types of NHK's cutting edge camera technology. For a high-spatial resolution, we have developed a Super Hi-vision (SHV) camera. SHV is our future TV broadcasting system and will realize greater sensation of reality. The camera system has 8k by 4k pixels at 60 frames-per-sec progressive scanning. For a high-temporal resolution, we have developed an ultrahigh-speed camera that provides one-million frames-per-sec. For a high-sensitivity, we have developed a Super HARP camera which sensitivity is fifty times higher than conventional CCD camera.

14:30-15:45 Session IV: Multicore and Image Processing
Co-Chairs: Tomochika Harada (Yamagata Univ.), Takashi Hashimoto (Panasonic)

14:30-14:55 **A 45nm Heterogeneous Multi-core SoC Supporting an over 32-bits Physical Address Space for Digital Appliance**
Takumi Nito[1], Yoichi Yuyama[2], Masayuki Ito[2], Yoshikazu Kiyoshige[2], Yusuke Nitta[2], Osamu Nishii[2], Atsushi Hasegawa[2], Makoto Ishikawa[1], Tetsuya Yamada[1], Junichi Miyakoshi[1], Koichi Terada[1], Tohru Nojiri[1],Masashi Takada[1], Makoto Satoh[1], Hiroyuki Mizuno[1], Kunio Uchiyama[1], Yasutaka Wada[3], Akihiro Hayashi[3], Keiji Kimura[3], Hironori Kasahara[3], Hideo Maejima[4] ([1]Hitachi, [2]Renesas Electronics, [3]Waseda Univ, [4]Tokyo Institute of Technology)

14:55-15:20 **A 36 Heterogeneous Core Architecture with Resource-aware Fine-grained Task Scheduling for Feedback Attention Based Object Recognition**
Seungjin Lee, Jinwook Oh, Minsu Kim, Joonyoung Park, Joonsoo Kwon, Joo-Young Kim, Hoi-Jun Yoo (KAIST, Korea)

15:20-15:45 **A High Throughput Hardware Architecture of Gaussian Mixture Model-based Classifier for Image Semantic Processing**
Yi-Ling Chen, Tse-Wei Chen, Shao-Yi Chien (National Taiwan Univ., Taiwan)

15:45-16:45 **Break (Poster Open: 7th floor poster show room)**

16:45-18:00 **Session V: Processor for Communication**
Co-chairs: Yuichiro Shibata (Nagasaki Univ.), Hiroyuki Igura (NEC)

16:45-17:10 **Low-power MIMO-OFDM Architecture with Dynamically Reconfigurable Hardware for Software-defined Radios**
Yohei Hasegawa, Fumihiko Hyuga, Masayuki Tokunaga, Yutaka Yamada, Takashi Yoshikawa, Shigehiro Asano (Toshiba)

17:10-17:35 **A 2Gbit/s Low-power Security Network Processor with a QoS Function for Residential Gateways**
Yukikuni Nishida, Kenji Kawai, Keiichi Koike (NTT)

17:35-18:00 **10G Ethernet iSCSI Protocol Controller with Companion Memory**
Atsushi Okamura, Takahiro Kawamura, Yasunori Kutsuma (Renesas Electronics)

April 16, 2010 *Main Hall(7th Floor), Yokohama Joho Bunka Center*
(Yokohama Media & Communications Center)

9:30-11:10 **Session VI**

9:30-10:20 **Keynote Presentation 4**
Co-chairs: Ryusuke Egawa (Tohoku Univ.), Yukinori Sato (JAIST)

Device Cloud Computing
Shih-Wei Liao (Google, USA)

Abstract: Targeting the audience at this chips conference, we will present a hardware-centric, end-to-end view of cloud computing: from the client side of the cloud computing to the data-center side of it. On the client side, we will present size optimizations for ROM/RAM and performance optimizations. The server side includes both the data center front-end and back-end. According to [Dean & Ghemawat] in CACM 2008, Google processed over 400 PB of data on datacenters composed of thousands of machines in September 2007 alone. What challenges emerge when computing on such a scale? We will describe some general, important advances at hardware level. Finally, we will discuss how cloud computing and client platforms amplify each other.

10:20-11:10 **Keynote Presentation 5**
Co-chairs: Kunio Uchiyama (Hitachi), Hiroaki Kobayashi (Tohoku Univ.)

NVIDIA Tegra, Architecture of Low Power
Gordon Grigor (NVIDIA, USA)

Abstract: Personal computers on are the brink of a technology change as devices move from stationary, to all day mobile platforms, where data is stored in the cloud. The consumer demand for mobile computing drives challenging requirements in terms of power and performance. Learn how holistic design created NVIDIA's Tegra to meet consumer needs.

11:10-11:30 **Break (Poster Open: 7th floor poster show room)**

11:30-12:20 **Session VII: Accelerators**
Co-chairs: Hoi-Jun Yoo (KAIST, Korea), Takeshi Kodaka (Toshiba)

11:30-11:55 **Multimedia System-on-a-chip: Low Power Multi-purpose GPU with Multi-core Stream Processor Unit and Universal Rasterizer and Mipmapping Texture Compression**
Chih-Hao Sun, You-Ming Tsao, Ka-Hang Lok, Shao-Yi Chien (National Taiwan Univ., Taiwan)

11:55-12:20 **An Energy-efficient Massively Parallel Embedded Processor Core for Real-time Image Processing SoC**
Hiroyuki Yamasaki, Takashi Kurafuji, Masaru Haraguchi, Tetsu Nishijima, Kan Murata, Tetsushi Tanizaki, Hideyuki Noda, Yoshihiro Okuno, Kazutami Arimoto (Renesas Electronics)

12:20-13:40 **Lunch Time Break**

13:40-14:30 **Session VIII**
Co-chairs: Makoto Ikeda (Univ. of Tokyo), Masato Suzuki (Panasonic)

13:40-14:30 **Keynote Presentation 6**

Sensors on Chips for Life Science Applications, Solutions for Fully-integrated Systems

Carlotta Guiducci (EPFL, Switzerland)

Abstract: The interface between electronic circuits and life sciences will be one of the focal points of future integrated system design. Several solutions for electronic devices/biological matter interactions are already available and they have proved their potential to be highly-portable systems or high-throughput systems or both.
In this speech, we will address the paradigm of electronic sensors, circuits and systems as privileged means to interact with biological matter at the higher level of detail while bringing the advantage of almost unlimited choice of signal processing, storing and communication solutions.
Sensing principles will be presented in a physics and biophysics perspective. High-throughput and integration will be addressed with respect to tradeoffs between high density and signal measurability.
A set of biomolecule sensing techniques and nanotechnological amplification means will be presented in their application in silicon-chip measurement systems.
The seminar will also tackle the compatibility issues of biochemical processes and solid-state technologies and will describe the different possibilities for developing and scale molecular sensing sites on a chip.

14:30-14:40 Break (Poster Open: 7th floor poster show room)

14:40-15:30 Session IX: Low Power Processor

Co-chairs: Kiat Seng Yeo (Nanyang Tech. Univ., Singapole), Kyoung-Rok Cho (Chungbuk National Univ., Korea)

14:40-15:05 **A Low Power SoC for Pressure Measurement Capsules in Ambulatory Urodynamic Monitoring**

Hirofumi Iwato, Keishi Sakanushi, Yoshinori Takeuchi, Masaharu Imai, Akira Matsuzawa, Yoshihiko Hirao (Osaka Univ.)

15:05-15:30 **Geyser-1 and Geyser-2 : MIPS R3000 CPU Chips with Fine-grain Runtime Power Gating**

Z.Lei[1], D.Ikebuchi[1], Y.Saito[1], M.Kamata[1], N.Seki[1], Y.Kojima[1], H.Amano[1], S.Koyama[2], T.Hashida[2], Y.Umahashi[2], D.Masuda[2], K.Usami[2], T.Sunata[3], K.Kimura[3], M.Namiki[3], S.Takeda[4], H.Nakamura[4], M.Kondo[5] ([1]Keio Univ., [2]Sibaura Institute of Technology, [3]Tokyo Univ. of Agriculture and Technology, [4]Univ. of Tokyo, [5]Univ. of Electro-Communications)

15:30-16:10 Session X

Co-chairs: Kazumasa Suzuki (Renesas Electronics), Yoshikazu Mori (Oki Network LSI)

15:30-16:10 **Invited Presentation**

Multi-Voltage Based Low Power Design Trends and Verification Techniques

Progyna Khondkar (Nihon Synopsys)

Abstract: Today's deep submicron semiconductor process technologies offer designers the ability to implement remarkably rich functionality in a very small die area. However, this result in increased high-frequency transistor switching and the resultant dynamic power dissipation directly impacts design reliability, battery life, packaging and cooling costs. In addition, with the migration to 65 nm process technologies and below, leakage power become just as problematic as dynamic power. In order to address dynamic and leakage power dissipation, designers must

incorporate various low power design techniques. Semiconductor physics show that voltage control is the key to reducing both dynamic and leakage power. Hence voltage control design techniques are becoming main stream which in turn impose varying degrees of new verification challenges, such as state-space complexity explosion, necessity of voltage aware simulation and power-aware assertions, as well checks for functional, structural and architectural changes in design due to protection cell insertion. Synopsys provides a distinct and unique approach to address low power verification challenges by combining tools and methodology. The Synopsys solution consists of voltage-aware simulation, a static checker that validates power intent throughout the design flow and an industry-first verification methodology based on best-practices from low power experts.

16:10-16:20 **Break**

16:20-18:20 **Session XI: Panel Discussions**
What is the future multi-layer co-design of computer systems?
Organizer & Moderator: Fumio Arakawa (Renesas Electronics)
Panelists: Jim Kahle (IBM, USA)
Shih-Wei Liao (Google, USA)
Chris Rowen (Tensilica, USA)
Srinivasan Murali (EPFL/iNoCs, Switzerland)
Ahmed Jerraya (CEA-LETI, France)
Iwao Yamazaki (Fujitsu)
Keiji Kimura (Waseda Univ.)

18:20-18:30 **Closing Remark**
Makoto Ikeda, Program Committee Co-chair (Univ. of Tokyo)