COOL Chips XIV Conference Time Table & Program (Final Ver.)
April 20-22, 2011 @ Yokohama Media & Communication Center, Yokohama, Japan

Wed. 20

Start	End	Duration	Session	Main Hall
13:00	15:30	2:30	Special Invited Lecture 1	**"Power Measurement, Characterization and Estimation of Microprocessor-Based Systems"** Naehyuck Chang (Seoul National University, Korea) Session Chair: Hiroyuki Tomiyama (Ritsumeikan Univ.) and Yuko Hara-Azumi (Ritsumeikan Univ.)
15:30	16:00	0:30	Break	
16:00	18:30	2:30	Special Invited Lecture 2	**"Trusted MpSoC platforms for safety related applications"** Rolf Ernst (Technische Universitat Braunschweig, Germany) Session Chair: Hiroyuki Tomiyama (Ritsumeikan Univ.) and Yuko Hara-Azumi (Ritsumeikan Univ.)

Thu. 21

Start	End	Duration	Session	Main Hall
9:30	9:50	0:20	Session I	Welcome & Opening Remarks
9:50	10:40	0:50	(continuation)	**Keynote Presentation 1** **"The Truths and Myths of Embedded Computing"** Shekhar Borkar (Intel, USA)
10:40	11:30	0:50	(continuation)	**Keynote Presentation 2** **"From Multi-Core CPU to Many-Core GPU"** Toru Baji (NVIDIA Japan) and Bill Dally (Chief Scientist & SVP of Research, NVIDIA)
11:30	11:40	0:10	Break	
11:40	12:10	0:30	Session II	**Poster Short Speech** Session Chair: Masanori Muroyama (Tohoku Univ., Japan)
12:10	13:30	1:20	Lunch	
13:30	14:20	0:50	Session III	**Keynote Presentation 3** **"Entering the Era of Crossover SoCs"** Patrick Lysaght (Xilinx, USA)
14:20	15:00	0:40	(continuation)	**Invited Talk 1** **"Full Software Implementation of Real-time ISDB-T Modulator on Dynamically Reconfigurable SoC Using Practical Co-design Environment"** Toru Awashima (Renesas Electronics Corp., Japan)
15:00	16:40	1:40	Break and Poster	
16:40	17:30	0:50	Session IV Session IV-1(R) Session IV-2(R)	**Reconfigurable Processors** Session Co-Chiars: Y. Kodama (Univ. of Tsukuba, Japan) and T. Hashimoto(Panasonic, Japan) **"FlexGripTM: A small and high-performance programmable hardware for highly sequential application"** T. Yoshikawa(Toshiba), F. Hyuga, M. Tokunaga, Y. Yamada, and S. Asano **"SLD-1(Silent Large Datapath): A Ultra Low Power Reconfigurable Accelerator"** N.Ozaki(Keio Univ.), Y.Yasuda, Y.Saito, D.Ikebuchi, M.Kimura, H.Amano, H.Nakamura, K.Usami, M.Namiki, and M.Kondo

17:30	18:10	0:40	Session V Session V-1(R) Session V-2(S)	**High-Performance Chip-to-Chip Interconnect** Session Co-Chiars: Y. Inoguchi (JAIST, Japan) and Y. Shibata (Nagasaki Univ., Japan) **"An 80Gb/s Dependable multicore Communication SoC with PCI Express I/F and Intelligent Interrupt Controller (Regular)"** S. Otani(Renesas), H. Kondo, I. Nonomura, A. Ikeya, M. Uemura, K.Asahina, K. Arimoto, S. Miura, T. Hanawa, T. Boku, and M. Sato **"COOL Interconnect Low Power Interconnection Technology for Scalable 3D LSI Design"** M. Chacin(TOPS Systems), H. Uchida, M. Hagimoto, T. Miyazaki, T. Ohkawa, R. Ikeno, Y. Matsumoto, F. Imura, M. Suzuki, K. Kikuchi, H. Nakagawa, and M. Aoyagi
18:10	18:30	0:20	Break	
18:30	20:30	2:00	Banquet	

Fri. 22

Start	End	Duration	Session	Main Hall
9:30	10:20	0:50	Session VI	**Keynote Presentation 4** **" AMD's Zacate, Low Power Fusion APU"** Denis Foley (Advanced Micro Devices, USA)
10:20	11:00	0:40	(continuation)	**Invited Talk 2** **"Advanced Machine Vision Technology Overcoming the Limits of Pixel Resolution"** Takafumi Aoki (Tohoku Univ., Japan)
11:00	11:10	0:10	Break	
11:10	12:05	0:55	Session VII Session VII-1(R) Session VII-2(S) Session VII-3(S)	**Low-Power Designs** Session Co-Chairs: K. Kimura (Waseda Univ., Japan) and H. Kawaguchi (Kobe Univ., Japan) **"A Low-Power Sync Processor with a Floating-Point Timer and Universal Edge Tracer for 3DTV Active Shutter Glasses"** D. Park(KAIST), T. G. Kim, C. Kim, and S. Kwak **"Loop-Directed Mothballing: Power-Gating Execution Units Using Fast Analysis of Inner Loops"** C. A. Court(Imperial College London) and P. H. J. Kelly **"A New Match Line Sensing Technique in Content Addressable Memory"** X-L. Tan(Nanyang Technological Univ.), A-T. Do, S-S. Chen, K-S. Yeo, and Z-H. Kong
12:05	13:15	1:10	Lunch	
13:15	14:05	0:50	Session VIII	**Keynote Presentation 5** **"Worldwide RMC Mobile Platform Solution"** Juha M. Heikkilä, (Renesas Mobile Corp., Finland)
14:05	14:45	0:40	(continulation)	**Invited Talk 3** **"The Correspondence between Architecture and Application for High Speed Vision Chips"** Masatoshi Ishikawa (Univ. of Tokyo, Japan)
14:45	14:55	0:10	Break	

14:55	15:50	0:55	Session IX Session IX-1(S) Session IX-2(R) Session IX-3(S)	**Wireless Baseband Architectures** Session Co-Chairs: K. -R. Cho (Chungbuk National Univ., Korea) and T. Kobori (NEC, Japan) **"Multi-Gbps 60-GHz Single-Carrier System Using a Low-Power Coherent Detection Technique)"** D. Nakano(IBM), Y. Kohda, K. Takano, T. Yamane, N. Ohba, and Y. Katayama **"A Multimodal Wireless Baseband Core using a Coarse-Grained Dynamic Reconfigurable Processor (Regular)"** H. Yamada(Toshiba), T. Yamagishi, T. Suzuki, K. Ito, K. Horisaki, T. V. Aa, T. Fujisawa, L. V. Perre, and Y. Unekawa **"A 7uW Deep-sleep, Ultra Low-power WLAN Baseband LSI for Mobile Applications"** D. Taki(Toshiba), T. Shiozawa, K. Ito, Y. Shiba, K. Horisaki, H. Kajihara, T. Yamagishi, M. Sekiya, A. Yamaga, T. Fujita, H. Hara, M. Kuwahara, T. Fujisawa, and Y. Unekawa
15:50	16:00	0:10	Break	
16:00	18:00	2:00	Session X	**Panel Discussion** **Topics: "Impact on society by fusion and harmony of mobile devices, servers, and networks -- Their direction of evolutions and optimal roles --"** Organizer & Modelator: Prof. Masato Motomura (Hokkaido Univ., Japan) Panelists: Toru Baji (NVIDIA Japan) Masatoshi Ishikawa (Univ. of Tokyo, Japan) Toru Awashima (Renesas Electronics Corp., Japan) Takafumi Aoki (Tohoku Univ., Japan) Toshihiro Hattori(Renesas Mobile Corp., Japan)
18:00	18:20	0:20		Closing Remarks

	Poster Program
Poster 1	**"Memory Array Based PLD Architecture for High-Density Logic Mapping – Implementation of First Demo Chip –"** Kazuya Tanigawa, Masanori Asaeda, Tetsuo Hironaka, Akihiro Yamada, Masayuki Sato, Takashi Ishiguro (Hiroshima City University, Japan)
Poster 2	**"Thermal-Aware Slack Distribution for Real-Time Systems"** Changha Lee, Young-Ho Lee and Jihong Kim (Seoul National University, Korea)
Poster 3	**"A Processor with Instruction Set Suitable for Extended Hamming Code"** Takashi Hamabe and Masaharu Imai (Osaka University, Japan)
Poster 4	**"A High Speed Design Using Divide-and-Conquer Architecture for Motion Estimation"** Shi-Yi Huang, Tsung-Yi Wu, You-Da Lin, Chien-Chih Lin, Tsung-Che Lee (National Changhua University of Education, Taiwan)
Poster 5	**"A Configurable Processor for Vascular Pattern Recognition"** G. T. Park and S. W. Kim (Korea University, Korea)
Poster 6	**"New Interconnection Network for Array Processors"** Abhijeet A. Ravankar and Stanislav G. Sedukhin (University of Aizu, Japan)
Poster 7	**Canceled**
Poster 8	**"3-Dimensional Network-on-Chip with Inductive coupling"** Daisuke Sasaki, Hiroki Matsutani, Yasuhiro Take, Yuki Ono, Yukinori Nishiyama, Tadahiro Kuroda, Hideharu Amano (Keio Univ, Japan)
Poster 9	**"Row-Based Power Gating on Functional Units"** Weihan Wang, Zhao Lei, Yuuya Outa, Kimiyoshi Usami, and Hideharu Amano (Keio Univ, Japan)
Poster 10	**"An Area Efficient Adaptive LUT Architecture"** Motoki Amagasaki, Kota Kato, Ken Taura, Masahiro Koga, Masahiro Iida and Toshinori Sueyoshi (Kumamoto University, Japan)
Poster 11	**"Implementation and Evaluation of a Low Power Accelerator SLD-2"** Mai Izawa, Nobuaki Ozaki, Yoshihiro Yasuda, Masayuki Kimura, Hideharu Amano (Keio Univ, Japan)
Poster 12	**"Instruction Gating for Low-Power Processor"** Seok-man Kim, Kwan-hee Lee and Kyoungrok Cho (Chungbuk Nat'l Univ, Korea)
Poster 13	**"Performance comparison of processors with different micro architectures"** Takayuki MATSUMURA, Yoshito SAKAGUCHI, Kenji KISE (Tokyo Institute of Technology, Japan)
Poster 14	**"Research on VLIW processors with fine-grained power gating"** Yoshifumi Ishii, Daisuke Ikebuchi, Hideharu Amano (Keio Univ, Japan)
Poster 15	**"Elimination of Execution Phases Using Pre-Execution"** Tsuyoshi MIKAMI, Yoshio SHIMOMURA and Ryotaro KOBAYASHI (Toyohashi University of Technology, Japan)
Poster 16	**"Power Saving of Value Prediction by Expanding Branch Target Buffer"** Yoshio SHIMOMURA and Ryotaro KOBAYASHI (Toyohashi University of Technology, Japan)
Poster 17	**"PEACH: A Communication SoC for PCI Express Direct Link"** Toshihiro Hanawa, Taisuke Boku, Shin'ichi Miura, Mitsuhisa Sato , and Kazutami Arimoto (University of Tsukuba, Japan)
Poster 18	**"Reduction method of refresh cycles for a dynamic optically reconfigurable gate array"** Yuji Aoyama and Minoru Watanabe (Shizuoka University, Japan)

Poster 19	**"GPU Implementation of Phase-Based Image Correspondence Matching and Its Evaluation"** Mamoru Miura, Kinya Fudano, Koichi Ito, and Takafumi Aoki (Tohoku Univ., Japan)
Poster 20	**"A Power-Aware Insertion Policy for the Way-Adaptable Cache Mechanism"** Yusuke Tobo, Masayuki Sato, Ryusuke Egawa, Hiroyuki Takizawa, and Hiroaki Kobayashi (Tohoku Univ., Japan)

–