COOL Chips XV Conference Time Table & Program (Ver. Apr. 2)
April 18-20, 2012 @ Yokohama Media & Communication Center, Yokohama, Japan

Wed. 18

Start	End	Duration	Session	Main Hall
13:00	15:30	2:30	Special Invited Lecture 1	**"Advanced Virtual Prototyping of Multiprocessor SoCs"** Frédéric Pétrot (TIMA Laboratory, France) Session Chair: Hiroyuki Tomiyama (Ritsumeikan Univ., Japan)
15:30	16:00	0:30	Break	
16:00	18:30	2:30	Special Invited Lecture 2	**"The Challenges of Analyzing Embedded Processor Behavior In the Age of Complex SoCs"** Markus Levy (EEMBC, USA) Session Chair: Hiroyuki Tomiyama (Ritsumeikan Univ., Japan)

Thu. 19

Start	End	Duration	Session	Main Hall
9:30	9:50	0:20		Welcome & Opening Remarks
9:50	10:40	0:50	Session I	**Keynote Presentation 1** **"The Expanding Universe of Embedded Imaging"** Masaki Hiraga (Morpho, Inc., Japan) Session Co-Chiars: R. Egawa (Tohoku Univ., Japan) and M. Ikeda (Univ. of Tokyo, Japan)
10:40	11:00	0:20	Break	
11:00	11:50	0:50	Session II Session II-1(R) Session II-2(R)	**Object Recognition** Session Co-Chiars: A. B.-Abdallah (Univ. of Aizu, Japan) and Y. Shibata (Nagasaki Univ., Japan) **"A Simultaneous Multithreading Heterogeneous Object Recognition Processor with Machine Learning Based Dynamic Resource Management,"** Jinwook Oh, Gyeonghoon Kim, Junyoung Park, Injoon Hong, Seungjin Lee, Joo-Young Kim, and Hoi-Jon Yoo (KAIST, Korea) **"Dual-Stage Hardware Architecture of On-Line Clustering with High-Throughput Parallel Divider for Low-Power Signal Processing,"** Tse-Wei Chen and Makoto Ikeda (Univ. of Tokyo, Japan)
11:50	12:30	0:40	Session III	**Poster Short Speech** Session Chair: K. Hashimoto (Fukuoka Univ., Japan)
12:30	14:00	1:30	Lunch	
14:00	14:50	0:50	Session IV	**Keynote Presentation 2** **"The IBM Blue Gene/Q Supercomputer,"** George Liang-Tai Chiu (IBM, USA) Session Co-Chiars: K. Takano (IBM, Japan) and Y. Nitta (Renesas, Japan)
14:50	16:20	1:30	Break and Poster	
16:20	18:20	2:00	Session V	**Panel Discussion** **Topics: "Technology exchange: Supercomputing and Embedded computing"** Organizer & Modelator: Hideharu Amano (Keio Univ, Japan) Panelists: TBA
18:20	18:40	0:20	Break	
18:40	20:40	2:00	Banquet	

Fri. 20

Start	End	Duration	Session	Main Hall
9:30	10:20	0:50	Session VI	**Keynote Presentation 3** **" Tofu Interconnect Controller for Fujitsu's Highly Scalable Supercomputer,"** Yuichiro Ajima (Fujitsu Ltd., Japan) Session Co-Chiars: Y. Hirose (Fujitsu Lab., Japan) and Y. Unekawa (Toshiba, Japan)
10:20	11:10	0:50	(Continuation)	**Keynote Presentation 4** **" Application Scalability - Key to Low Power, Performance Growth, and Exascale,"** Wen-mei Hwu (Illinois Univ., USA) Session Co-Chiars: H. Takizawa (Tohoku Univ., Japan) and A. Hashiguchi (SONY, Japan)
11:10	11:30	0:20	Break	
11:30	12:20	0:50	Session VII	**3D Integration** Session Co-Chiars: H. Yamada (Hitachi, Japan) and T. Harada (Yamagata Univ., Japan)
			Session VII-1(R)	**"A 5.184Gbps/ch Through-Chip Interface and Automated Place-and-Route Design Methodology for 3-D Integration of 45nm CMOS Processors,"** Yasuhisa Shimazaki, Noriyuki Miura, and Tadahiro Kuroda (Renesas, Japan)
			Session VII-2(R)	**"Cool System Scalable 3-D stacked Heterogeneous Multi-Core / Multi-Chip Architecture for Ultra Low-Power Digital TV Applications,"** Yukoh Matsumoto, Tomoyuki Morimoto, Michiya Hagimoto, Hiroyuki Uchida, Nobuyuki Hikichi, Fumito Imura, Hiroshi Nakagawa, and Masahiro Aoyagi(TOPS Systems, Japan)
12:20	13:50	1:30	Lunch	
13:50	14:40	0:50	Session VIII	**Keynote Presentation 5** **"Nonvolatile Logic-in-Memory Architecture Using an MTJ/MOS-Hybrid Structure and Its Applications,"** Takahiro Hanyu (Tohoku Univ., Japan) Session Co-Chiars: K. Suzuki (Renesas, Japan) and H. Igura (NEC, Japan)
14:40	14:50	0:10	Break	
14:50	16:05	1:15	Session IX	**Power Gating and Circuit** Session Co-Chiars: K. -R. Cho (Chungbuk National Univ., Korea) and S. Otani (Renesas, Japan)
			Session IX-1(R)	**"Gate-level Process Variation Offset Technique by using Dual Voltage Supplies to Achieve Near-threshold Energy Efficient Operation,"** Benjamin Devlin, Makoto Ikeda, and Kunihiro Asada (Univ. of Tokyo, Japan)
			Session IX-2(R)	**"An Area-Efficient, Standard-Cell Based On-Chip NMOS and PMOS Performance Monitor for Process,"** Toshiyuki Yamagishi, Tatsuo Shiozawa, Koji Horisaki, Hiroyuki Hara and and Yasuo Unekawa (Toshiba, Japan)
			Session IX-3(S)	**"Trade-off Analysis of Fine-grained Power Gating Methods for Functional Units in a CPU,"** Weihan Wang, Yuya Ohta, Yoshifumi Ishii, Kimiyoshi Usami, and Hideharu Amano (Keio Univ./ Shibaura Inst. Tech., Japan)
16:05	16:20	0:15	Break	
16:20	17:10	0:50	Session X	**Processor** Session Co-Chiars: J. Yao (NAIST, Japan) and Y. Kodama (Univ. of Tsukuba, Japan)
			Session IX-1(R)	**"A Media-oriented Vector Architectural Extension with a High Bandwidth Cahe System,"** Ye Gao, Naoki Shoji, Ryusuke Egawa, Hiroyuki Takizawa, and Hiroaki Kobayashi (Tohoku Univ., Japan)
			Session IX-2(R)	**"Dependable Responsive Multithreaded Processor for Distributed Real-Time Systems,"** Kazutoshi Suito, Kei Fujii, Hiroki Matsutani, and Nobuyuki Yamasaki (Keio Univ., Japan)

17:10	17:40	0:30	(Continuation)	**Special Invited talk** **"Seahawk - Optimizing power efficiency in high performance Cortex-A15 processor implementations,"** Dermot O'Driscoll and Sumit Sahai (ARM, U.K.) Session Co-Chiars: J. Yao (NAIST, Japan) and Y. Kodama (Univ. of Tsukuba, Japan)
17:40	18:00	0:20		Poster Award and Closing Remarks

	Poster Program
Poster 1	**"Energy Saving of BTB by Focusing on Useless References,"** Yoshio Shimomura, Hayato Usui, Genta Abe, and Ryotaro Kobayashi (Toyohashi Univ. of Tech., Japan)
Poster 2	**"A Reduction Technique of Static Power Consumption of Scratch-Pad Memory by Dynamic Switching of SPM Block,"** Shoma Kawai, Takashi Morimoto, and Ryotaro Kobayashi (Toyohashi Univ. of Tech., Japan)
Poster 3	**"A Preliminary Study on Reducing Cache Size by Focusing on Data Redundancy,"** Daisuke Matsukawa, Yoshio Shimomura, and Ryotaro Kobayashi (Toyohashi Univ. of Tech., Japan)
Poster 4	**"A Preliminary Study on Value Consistency for Preload,"** Kazuki Sekikawa, Hayato Usui, Yoshio Shimomura, and Ryotaro Kobayashi (Toyohashi Univ. of Tech., Japan)
Poster 5	**"A Low Power SRAM Design with Segmented Stacking Technique,"** Shuang-An Tseng, Tung-Chi Wu, and Yen-Jen Chang (National Chung Hsing Univ., Taiwan)
Poster 6	**"Synthesis and Implementation of Low Power Logic Cells,"** Tsung-Yi Wu, Tai-Lun Li, and Hao-Lung Hsueh (National Changhua Univ. of Education, Taiwan)
Poster 7	**"High-Performance Low-Power Motion Estimation Algorithm and C Code for ATmega328 and ARM Cortex-M3,"** Tsung-Yi Wu, Tsung-Che Lee, and Yu-Sheng Wu (National Changhua Univ. of Education, Taiwan)
Poster 8	**"Low-Area, High-Speed Logarithmic and Anti-logarithmic Converters for Digital Signal Processors Based on Hybrid Number System,"** Van-Phuc Hoang and Cong-Kha Pham (Univ. of Electro-Communications, Japan)
Poster 9	**"A Branch Target Address Predictor for Reducing the BTB Miss by Using CAM,"** Lin Meng, Takeshi Kumaki, Katsuhiro Yamazaki, Takeshi Ogura, and Shigeru Oyanagi (Ritsumeikan Univ., Japan)
Poster 10	**"Co-design of the Extremely Scalable Algorithms/Architecture for 3D Discrete Transforms,"** Stanislav G. Sedukhin, Toshiaki Miyazaki, and Kenichi Kuroda (Univ. of Aizu, Japan)
Poster 11	**"A Bypass Mechanism for Way-Adaptable Caches,"** Takumi Takai, Yusuke Tobo, Masayuki Sato, Ryusuke Egawa, Hiroyuki Takizawa, and Hiroaki Kobayashi (Tohoku Univ., Japan)
Poster 12	**"Application Development for a Heterogeneous Multi-Core Processor,"** Yusuke Koizumi, Eiichi Sasaki, Mitaro Namiki, and Hideharu Amano (Keio Univ./ Tokyo Univ. of Agri. & Tech., Japan)
Poster 13	**"Design Exploration of PE Array Networks for Cool Mega Array,"** Rie Uno, Nobuaki Ozaki, and Hideharu Amano (Keio Univ., Japan)
Poster 14	**"Extension of memory controller equipped with MuCCRA-3,"** Toru Katagiri, Kazuei Hironaka, and Hideharu Amano (Keio Univ., Japan)

Poster 15	**"A Fine-Grained Power Gating Control for a Real Time Operating System,"** Yumi Shimada, Hiroaki Kobayashi, Akihiro Takahashi, Ryuiti Sakamoto, Mikiko Sato, Masaaki Kondo, Hideharu Amano, Hiroshi Nakamura, and Mitaro Namiki (Tokyo Univ. of Agri. & Tech./ Univ. of Electro-Communication/ Keio Univ./ Univ. of Tokyo, Japan)
Poster 16	**"A Hardware Edge Detector of an Image Based on a Bump Circuit and the Neighbor Pixels,"** Kwang-Seok Oh , Sang-Jin Lee, and Kyoungrok Cho (Chungbuk National Univ., Korea)
Poster 17	**"Application of SerDes for FPGA-based digital DC-DC Converters,"** Yoshihiko Yamabe, Kanako Nakashima, Keisuke Dohi, Kazuhiro Kajiwara, Fujio Kurokawa, and Yuichiro Shibata (Nagasaki Univ., Japan)
Poster 18	**"A Design Methodology for High-Performance D/A Converter utilizing Optimized Weights,"** Daisuke Kanemoto, Haruichi Kanaya, Keiji Yoshida, and Ramesh Pokharel (Kyushu Univ., Japan)
Poster 19	**"Enhancing Simulation Performance of Network-on-Chip by Using Multi-core Systems,"** Kuei-Chung Chang (Feng Chia Univ., Taiwan)
Poster 20	**"Simple On-chip Optical Interconnection for Improving Performance of Coherency Traffic in CMPs,"** Sandro Bartolini and Paolo Grani (University of Siena, Italy)
Poster 21	**"Distributed Computing Circuits in Scalable 2D/3D FPGA Array for 2D/3D Poisson Equation Problem,"** Jiang Li, Kenichi Takahashi, Hakaru Tamukoh, and Masatoshi Sekine (Tokyo Univ. of Agri. & Tech., Japan)
Poster 22	**"Scheduling Sensor IO for Minimizing Battery Consumption and Voltage Drop in Sensor Node,"** Qian Zhao, Shimpei Yamada, Yukikazu Nakamoto (Univ.of Hyogo, Japan), Koutaro Yamamura, Makoto Iwata, and Masayoshi Kai (NEC System Technologies, Japan)

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