COOL Chips XVI Final Program

April 17, 2013 *Main Hall(7th Floor), Yokohama Joho Bunka Center*
(Yokohama Media & Communications Center)

13:00-15:30 **Special Session 1**
Chair: Hiroyuki Tomiyama (Ritsumeikan University)

13:00-15:30 **STHORM: A Multi-Processor Platform and Programming Environment**
Speaker: Pierre G. Paulin (STMicroelectronics, Canada)

Abstract: In this talk we will present the STMicroelectronics STHORM* multi-processor fabric and its programming environment. (* formerly known as Platform 2012)

- STHORM many-core platform overview
  - Multi-cluster and multi-core platform
  - Asynchronous Network-on-Chip
  - Memory hierarchy and DMA
  - STHORM SoC
- Platform programming model (PPM) support:
  - OpenCL: Standard PPM for S/W-based platform variants
  - Native Programming Model (NPM): A flexible, open source component-based environment and runtime for programming model experimentation.
  - Predicated Execution Data Flow (PEDF), for mixed HW-SW platform variants
- Programming model-aware debug, trace, visualization and analysis tools
- STHORM platforms
  - Virtual platform: Functional and performance models
  - STHORM evaluation board
- Application and benchmarking results
  - Focus on computer vision and augmented reality applications
  - Application library, integrated in OpenCV and Android environments
  - Benchmark comparison with general-purpose processor

15:30-16:00 **Break**

16:00-18:30 **Special Session 2**
Chair: Hiroyuki Tomiyama (Ritsumeikan University)

16:00-18:30 **Hot Research Issues in Main Memory Subsystem**
Speakers: Jung Ho Ahn (Seoul National University, Korea), Sungjoo Yoo (POSTECH, Korea)

Abstract: DRAM has served as a de facto standard for main memory for decades owing to its low-latency and high-density features. Recently, the power and latency of its inter-package and on-chip global datalines has become the primary inhibitors in further improving the performance and energy-efficiency of the main-memory systems. 3D stacking technologies, such as through-silicon via, have been suggested and adopted to alleviate the problem by lowering the impedance and physical distance between storage and computation components. In this talk, we first survey the solution space of 3D stacked DRAM systems from industry and academia. After reviewing their recent progresses, we identify the active issues in developing and utilizing the 3D stacked DRAM systems. In the long-term,

emerging memory technologies can resolve the scaling problem of DRAM. We focus on a promising emerging memory, phase-change RAM (PRAM). First, we present an overview of recent research work on applying PRAM to the main memory subsystem. Then, we explain key solutions in the topics of hybrid DRAM/PRAM, data encoding for bit update reduction, wear leveling, error correction, and write performance improvement. Finally, we present current issues to realize multi-level cell PRAM which is imperative to realize low bit-cost in PRAM.

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9:30-9:50 **Session I**

9:30-9:50 **Welcome and Opening Remarks**
Chair: Kazumasa Suzuki (Renesas Electronics)

Hiroaki Kobayashi,	*Chair of the Organizing Committee*
Donald. A. Draper,	*Chair of TCMCOMP*
Kiyomichi Araki,	*President of Electronics Society, IEICE*
Fumiko Hayashi,	*Mayor of Yokohama City*

9:50-11:30 **Session II**

9:50-10:40 **Keynote Presentation 1**
Co-chairs: Masato Suzuki (Panasonic), Yukinori Sato (JAIST)

What Can Supercomputers Learn from Phones?
Michael McCool (Intel, USA)

Abstract: Energy efficiency and power management have become crucial factors in all forms of computation, from phones to supercomputers, and Intel produces processors for the entire range. Phones, with their limited thermal and battery power budgets, need careful management of power consumption driven by the specific use-case scenarios in which these devices are used. For example, mobile applications are frequently very "bursty" in nature and it is possible to temporarily exceed the thermal budget of the device and race to halt, improving both the user experience (since the task is completed faster) and lowering the overall system power requirements (since the display and other components can be turned off sooner). A great deal of effort also goes into systems management in phones so that features not actually needed for a specific task can be powered down, and so that the minimum processor power needed for the task can be used. Supercomputer applications also have limited power budgets. Targets for Exascale computing in particular emphasize not only raw performance, but achieving that performance within a specific system power budget. Compared with phones, supercomputers are used for continuous operation, and so the strategies used for power management are different---or are they? What can we learn from phones to optimize power consumption in supercomputers? In this talk I will review the power management facilities in Intel processors across the compute continuum, their evolution, convergence, and divergence, and point out some interesting research opportunities.

10:40-11:30 **Keynote Presentation 2**
Co-chairs: Kazumasa Suzuki (Renesas Electronics), Hiroyuki Igura (NEC)

Next Generation Vector Supercomputer for Providing Higher Sustained Performance
Shintaro Momose (NEC)

Abstract: Many of the current supercomputers are designed to target higher peak performance with lower memory bandwidth due to the memory wall issue. However, the characteristics of applications in the High Performance Computing (HPC) area are getting diversified and the sustained performance of each application strongly depends on not only the peak performance of the system but also its memory bandwidth. The NEC's goal is to provide higher sustained performance for

every application area with the vector supercomputer for memory-intensive applications and with commodity products such as x86-based clusters and accelerators for compute-intensive applications. Within a year, we are going to launch the Next Generation Vector Supercomputer (NGV) aimed at much higher sustained performance particularly for memory intensive applications, which is the successor model of our current SX-9 products. NGV is designed with the big core strategy targeting higher sustained performance in parallel execution and improved programmability/productivity for users. NGV has both the world highest single core performance of 64GF and the world highest memory bandwidth per core of 64GB/s. Four cores, memory controllers and network controllers are integrated into one CPU LSI, enabling the CPU performance of 256GF and the memory bandwidth of 256GB/s. NEC is also participating in the feasibility study of future HPC technologies as part of the Japanese governmental HPCI project with Tohoku University and JAMSTEC. Our target will remain unchanged with the big core-based design balanced with large memory bandwidth over 1 Byte/Flop, pursuing higher sustained performance (not Linpack) for the enhanced applicability to disaster prevention/mitigation and industrial applications.

11:30-11:40 **Break**

11:40-12:10 **Session III : Poster Short Speeches**
Chair: Koji Hashimoto (Fukuoka University)

Poster 1 **Dalvik VM JIT Compiler for Fine-Grained Power Gating Control**
Motoki Wada[1], Jun Tsukamoto[1], Hiroaki Kobayashi[1], Akihiko Takahashi[1], Ryuichi Sakamoto[1], Mikiko Sato[1], Masaaki Kondo[2], Hideharu Amano[3], Hiroshi Nakamura[3], Mitaro Namiki[1] ([1]Tokyo University of Agriculture and Technology, [2]University of Electro-Communication, [3]Keio University, [4]University of Tokyo)

Poster 2 **A Basic Study on Leakage Power Reduction for FPU by Fine-grained Power Gating Control**
Jun Tsukamoto[1], Motoki Wada[1], Yumi Shimada[1], Ryuichi Sakamoto[1], Mikiko Sato[1], Masaaki Kondo[2], Kimiyoshi Usami[3], Hideharu Amano[4], Hiroshi Nakamura[5], Mitaro Namiki[1] ([1]Tokyo University of Agriculture and Technology, [2]University of Electro-Communication, [3]Shibaura Institute of Technology, [4]Keio University, [5]University of Tokyo)

Poster 3 **Reducing Cache Size by Focusing on Frequent Higher Bits**
Hiroya Ochiai[1], Daisuke Matsukawa[1], Yoshio Shimomura[1], Ryotaro Kobayashi[1], Hajime Shimada[2] ([1]Toyohashi University of Technology, [2]Nara Institute of Science and Technology)

Poster 4 **ALU Cascading Based on Different Execution Latencies of Each Instruction**
Hiroki Yamamoto[1], Kazuki Sekikawa[1], Ryotaro Kobayashi[1], Hajime Shimada[2] ([1]Toyohashi University of Technology, [2]Nara Institute of Science and Technology)

Poster 5 **Improve Efficiency of Return Address Stack Using Decode Information**
Mizuki Watanabe[1], Hayato Usui[1], Yoshio Shimomura[1], Ryotaro Kobayashi[1], Hajime Shimada[2] ([1]Toyohashi University of Technology, [2]Nara Institute of Science and Technology)

Poster 6 **High-Speed Block Cipher, HIGHT for RFID in VHF Band**
Je-Hoon Lee, Young-Min Song, Si-Byung Nam, Sang-Choon Kim, Duk-Gyu Lim (Kangwon National University)

Poster 7 **The Early Prediction of On-chip Bus Latency with Fixed-Priority Arbitration Policy**

Poster 21 **An Implementation of Common Mode Free and New Switching Scheme SAR ADC**
Daisuke Kanemoto[1], Keigo Oshiro[2], Haruichi Kanaya[2], Keiji Yoshida[2] ([1]Yamanashi University, [2]Kyushu University)

Poster 22 **Image Processing Hardware Design Framework and FPGA Implementation by Hierarchical Models**
Katsunori Hirano[1], Yuichi Sakurai[1], Tadanobu Toba[1], Masashi Watanabe[2], Yoshinobu Hoshino[2] ([1]Hitach, [2]Hitachi High-Technologies)

Poster 23 **Towards An Energy-Efficient Scheduler in the Codelet Model**
Kotoko Fujita[1], Nadav Bergstein[1], Hakaru Tamukoh[2], Masatoshi Sekine[1] ([1]Tokyo University of Agriculture and Technology, [2]Kyushu Institute of Technology)

Poster 24 **A TCP/IP Hardware Stack Directly Connectable to WEB Application Circuit**
Kotoko Fujita[1], Nadav Bergstein[1], Hakaru Tamukoh[2], Masatoshi Sekine[1] ([1]Tokyo University of Agriculture and Technology, [2]Kyushu Institute of Technology)

Poster 25 **Parallel Processing of Multimedia Applications on TILEPro64**
Yohei Kishimoto[1], Hiroki Mikami[1], Keiichi Nakano[2], Akihiro Hayashi[1], Keiji Kimura[1], Hironori Kasahara[1] ([1]Waseda University, [2]Olympus Corporation)

Poster 26 **SMYLEvideo: Distributed Processing on Scalable Heterogeneous Manycore Architecture for Video Mining Applications**
Sunao Torii, Michiya Hagimoto, Hiroyuki Uchida, Masamichi Izumida, Yukoh Matsumoto (TOPS Systems)

12:10-13:10 Lunch Time Break

13:10-13:30 Poster Open: 7th floor poster show room

13:30-14:20 Session IV
Co-chairs: Akihiko Hashiguchi (Sony), Yasuo Unekawa (Toshiba)

13:30-14:20 **Keynote Presentation 3**
CoolChips at the core of a healthier world
Bert Gyselinckx (IMEC, Netherlands)

Abstract: A healthier world ... is that not what we all wish for in our new year's resolutions? So why is it then that so many people suffer from disease that is caused be lifestyle choices. There are many ways to approach this question. In this talk, we take the stance that people have a strong trust in the incumbent healthcare system and under estimate the impact daily behavior can have on the longer term. As a result we are seeing pandemics of chronic disease that are saturating our healthcare systems and driving the costs through the roof. Technology cannot change the world, only people can. But technology can help people change the world. Biochemical progress has equipped us with drugs that can cure disease. Engineering and physics have brought us very advanced imaging systems that can look inside us without using a scalpel. Now we are ready for the next step. Technology that can help us with making lifestyle changes. Technology that will help us manage our health. And in the odd event that we do get ill, the same technology will help us to get on our feet as fast as possible. The magic ingredient for all of this, is the body area network. Think of it as an aura of invisible health guards. These health guards are embedded in clothing, jewelry, or eyewear and communicate with the cloud through a mobile device. This revolution is happening today. Many players are introducing cardiac, brain, sleep, or energy expenditure monitoring systems. This is

just a first step of this new wave. Cool chips, chips that are very small and hardly consume any power will allow to further miniaturize such systems. This will lead to throughly pervasive BAN systems. In 10 years time, we will all be walking around with embedded health guards, like we are carrying around our cell phones today. In 10 years time, we will manage our own health. Or, we will at least be better equipped to do so if we want.

14:20-15:20 **Break (Poster Open: 7th floor poster show room)**

15:20-16:00 **Session V**
Co-chairs: Hideharu Amano (Keio University), Fumio Arakawa (Renesas Electronics)

15:20-16:00 **Invited Presentation 1**
Zero Overhead State-Retention Power-Gating and Gate-Bias on a Dual-Core ARM Cortex-A5MP Processor for 50-80% Idle Power Reduction
James Myers (ARM, UK)

Abstract: Power gating is now a mainstream leakage mitigation technique implemented in all modern SoCs, but saving away program state and actually shutting down is an energy gamble left to the Operating System. Hardware state retention registers allow more opportunity for power gating with less software, energy and latency overhead. A dual-core ARM® processor is fabricated on a 65nm process with zero-area retention, along with on-chip voltage reduction circuitry, which enables five intermediate power modes of gradually increasing leakage reduction and wake latency. Leakage savings between 50-80% are observed at room temperature.

16:00-16:50 **Session VI: Low Power Processors**
Co-chairs: Abderazek Ben-Abdallah (University of Aizu), Kotaro Shimamura (Hitachi)

16:00-16:25 **Processor with 4.9-us Break-even Time in Power Gating Using Crystalline In-Ga-Zn-Oxide Transistor**
Hidetomo Kobayashi, Kiyoshi Kato, Takuro Ohmaru, Seiichi Yoneda, Tatsuji Nishijima, Shuhei Maeda, Kazuaki Ohshima, Hikaru Tamura, Hiroyuki Tomatsu, Tomoaki Atsumi, Yutaka Shionoiri, Yukio Maehashi, Jun Koyama, Shunpei Yamazaki (Semiconductor Energy Laboratory)

16:25-16:50 **RXv2 processor core for low-power microcontrollers**
Sugako Otani, Hiroyuki Kondo, Naoshi Ishikawa (Renesas Electronics)

16:50-17:00 **Break**

17:00-18:40 **Session VII: Panel Discussions**
Topics: The Next Step in Processor Evolution
Organizer & Moderator: Yoshio Masubuchi (Toshiba)
Panelists: Bert Gyselinckx (IMEC, Netherlands)
Michael McCool (Intel, USA)
Shintaro Momose (NEC)
James Myers (ARM, UK)
Toshio Yoshida (Fujitsu)

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9:30-11:00 **Session VIII**

9:30-10:20 **Keynote Presentation 4**
Co-chairs: Kohji Takano (IBM), Makoto Ikeda (University of Tokyo)

Why and how "Watson" Answered Questions on the TV Quiz Show?
Hiroshi Kanayama (IBM Japan)

Abstract: IBM Research decided to build a question answering system, Watson, to compete with humans on the American TV Quiz show, Jeopardy! We improved Natural Language Processing (NLP), Information Retrieval (IR), Machine Learning (ML), massively parallel computation and Knowledge Representation and Reasoning (KR&R), and created an architecture to integrate all of them, and the resulting system competed on television against two famous human champions on an equal footing. Our results proved that our architecture is effective and extensible and may be used as a foundation for combining, deploying, evaluating and advancing a wide range of algorithmic techniques to rapidly advance the field of open domain question answering. In this talk I will introduce the grand challenge, present an overview of the technology upon which Watson is built, including hardware points of view, and explore how the technology is being applied to new industries and domains, such as healthcare.

10:20-11:00 **Invited Presentation 2**
Co-chairs: Yoshio Hirose (Fujitsu Laboratories), Ryusuke Egawa (Tohoku University)

SPARC64™ X: Fujitsu's New Generation 16 Core Processor for UNIX servers
Toshio Yoshida (Fujitsu)

Abstract: Fujitsu has developed a new processor SPARC64™ X for UNIX server, which runs at a speed of 3GHz and consists of 16 cores, a 24MB shared level 2 cache, memory controllers, IO controllers and system controllers which connect multiple chips. We have strengthened a microarchitecture and introduced the enhanced instruction sets HPC-ACE (High performance computing-arithmetic computational extensions), which have been already applied to the K computer. Peak memory bandwidth reaches 102GB/s. An extremely high throughput performance is realized by those features. In addition, we have added new functions to the core pipelines, which accelerate software such as cryptography processing and some specific applications. We call these architectures 'Software on Chip.' Furthermore, high-reliability technology for mainframes is used to ensure stable operation of a mission-critical system. This presentation will introduce the overview of SPARC64TM X, performance and power efficiency of 'Software on Chip.'

11:00-11:20 **Break (Poster Open: 7th floor poster show room)**

11:20-12:35 **Session IX: Many-Core Processors**
Co-chairs: Byeong-Gyu Nam (Chungnam National University), Hajime Shimada (Nara Institute of Science and Technology)

11:20-11:45 **A Scalable 3D Heterogeneous Multi-Core Processor with Inductive-Coupling ThruChip Interface**

Noriyuki Miura, Yusuke Koizumi, Eiichi Sasaki, Yasuhiro Take, Hiroki Matsutani, Tadahiro Kuroda, Hideharu Amano, Ryuichi Sakamoto, Mitaro Namiki, Kimiyoshi Usami, Masaaki Kondo, Hiroshi Nakamura (Keio University)

11:45-12:10 **A multi-granularity parallelism object recognition processor with content-aware fine-grained task scheduling**
Junyoung Park, Injoon Hong, Gyeonghoon Kim, Youchang Kim, Kyuho Lee, Seongwook Park, Kyeongryeol Bong, Hoi-Jun Yoo (KAIST)

12:10-12:35 **Power Efficient Realtime Super Resolution by Virtual Pipeline Technique on a Server with Manycore Coprocessors**
K. Ishizaka, T. Miyamoto, S. Akimoto, A. Iketani, T. Hosomi, J. Sakai (NEC)

12:35-13:55 Lunch Time Break

13:55-14:35 Session X
Co-chairs: Yusuke Nitta (Renesas Electronics), Koyo Nitta (NTT)

13:55-14:35 **Invited Presentation 3**
A 28nm HKMG Single-Chip Communications Processor with 1.5GHz Dual-Core Application Processor and LTE/HSPA+ Capable Baseband Processor
Takeshi Kataoka (Renesas Mobile)

Abstract: The R-Mobile U2 (RMU2) achieves single-chip integration of 1.5GHz dual core application processor and 2G/3G/HSPA+/LTE baseband processor by 28nm HKMG High-Performance and Low-Leakage CMOS bulk process, which satisfies low leakage current and high performance. Additionally, this chip features a clock control mechanism “Power Saver” to limit maximum power and to reduce IR drop in short term. This chip also features IO NMOS power switch and Dual Mode Low-leak SRAM to minimize leakage current.

14:35-15:50 Session XI: HW/SW Technologies
Co-chairs: Hiroyuki Takizawa (Tohoku University), Yuetsu Kodama (University of Tsukuba)

14:35-15:00 **Automatic Parallelization, Performance Predictability and Power Control for Mobile-Applications**
Dominic Hillenbrand, Akihiro Hayashi, Hideo Yamamoto, Keiji Kimura, Hironori Kasahara (Waseda University)

15:00-15:25 **HW/SW Approaches to Accelerate GRAPES in an FU Array**
Wei Wang, Jun Yao, Youhui Zhang, Wei Xue, Yasuhiko Nakashima, Weimin Zheng (Tsinghua University, China)

15:25-15:50 **Parallelization of Automotive Engine Control Software On Embedded Multi-core Processor Using OSCAR Compiler**
Yohei Kanehagi, Dan Umeda, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara (Waseda University)

15:50-16:10 Break (Poster Open: 7th floor poster show room)

16:10-17:00 Session XII: Resource Management
Chair: Jun Yao (Nara Institute of Science and Technology)

16:10-16:35 **Hardware Support for Resource Partitioning in Real-Time Embedded Systems**
Tetsuro Honmura, Yuki Kondoh, Tetsuya Yamada, Masashi Takada, Takumi Nitoh, Tohru Nojiri, and Keisuke Toyama, Yasuhiko, Saitoh, Hirofumi Nishi, Mikiko Sato,

Mitaro Namiki (Hitachi)

16:35-17:00 **A Flexible Insertion Policy for Dynamic Cache Resizing Mechanisms**
Masayuki Sato, Yusuke Tobo, Ryusuke Egawa, Hiroyuki Takizawa, Hiroaki Kobayashi (Tohoku University)

17:00-17:50 Session XIII: 3D Technologies
Co-chairs: Yuichiro Shibata (Nagasaki University), Yasutaka Wada (NEC)

17:00-17:25 **Dynamic Power On/Off Method for 3D NoCs with Wireless Inductive-Coupling Links**
Hao Zhang, Hiroki Matsutani, Michihiro Koibuchi, Hideharu Amano (Keio University)

17:25-17:50 **Architecture Level TSV Count Minimization Methodology for 3D Tree-based FPGA**
Vinod Pangracious, Habib Mehrez, Zied Marakchi (University of Pierre and Marie Curie Paris, France)

17:50-18:10 Poster Award and Closing Remark
Makoto Ikeda, Program Committee Co-chair (University of Tokyo)